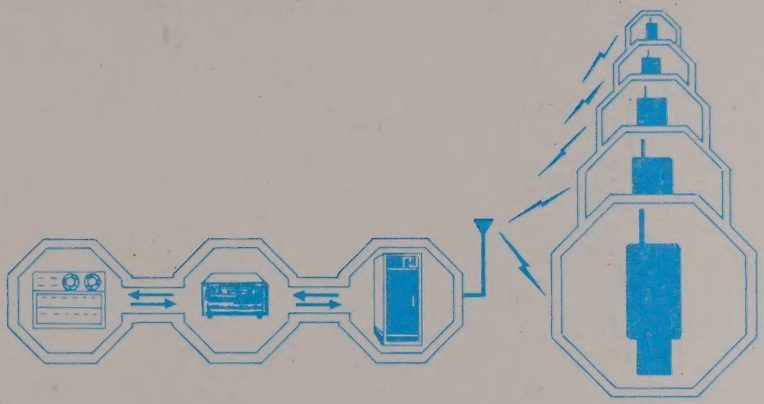
MOTOROLA

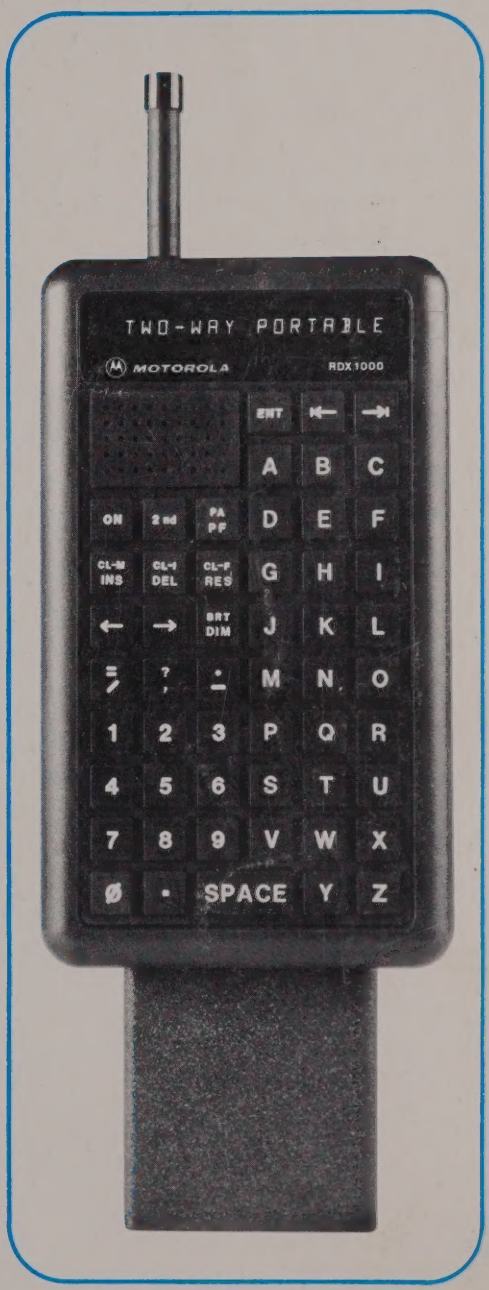
RDX 1000

Portable RF Data Terminals

403-430, 440-512 MHz

MODELS N1257A, N1258A





Instruction Manual

68P81014C65-A

FOREWORD

SCOPE OF INSTRUCTION MANUAL

This manual offers descriptive data and service information for the equipment listed. Service diagrams, parts lists, and printed circuit board details are either a part of this instruction manual, or are contained in a supplementary service manual.

NOMENCLATURE

Motorola equipment is specifically identified by the model number on the nameplate.

NOTE: Be sure to use the entire model number when making inquiries about your equipment.

Identifiers have been assigned to chassis and kits. Use these identifiers when requesting information or ordering replacements.

PRODUCTION CHANGES

When production and engineering changes are incorporated into the equipment, a revision number is assigned to the chassis or kit affected; -1, -2, -3, etc.

The chassis number complete with revision number, if any, is stamped on the chassis at the time of production. The revision number becomes an integral part of the chassis identifier. Revisions, if any, are listed on the schematic diagram.

INSTRUCTION MANUAL REVISIONS

Changes which occur after an instruction manual is printed are described in the Instruction Manual Revision. These bulletins give the reader complete information on the change including pertinent parts listing data.

NATIONAL SERVICE ORGANIZATION

Motorola provides a nationwide service organization. Through its maintenance and installation program, Motorola makes available the finest service to those desiring reliable continuous communications on a contract basis.

Motorola's National Service Organization is the largest service organization specializing in mobile communications. It includes over 800 independently owned and operated service stations, strategically located and manned by a staff of several thousand FCC licensed personnel.

The area administrative staff, district service managers, and district service representatives are in the direct employ of Motorola.

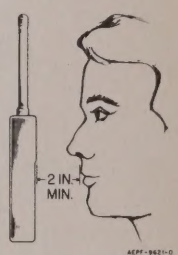
For your contract service requirements, please contact your local Motorola representative or write to:

National Service Manager
Motorola Communications & Electronics, Inc.
1301 Algonquin Road, Schaumburg, IL 60196

SAFETY INFORMATION

The United States Department of Labor, through the provisions of the Occupational Safety and Health Act of 1970 (OSHA), has established an electromagnetic energy safety standard which applies to this equipment. Proper use of this radio will result in exposure below the OSHA limit.

DO NOT hold the radio with the antenna very close to, or touching, exposed parts of the body, expecially the face or eyes, while transmitting. The radio will perform best if the microphone is two or three inches away from the lips and the radio is vertical.



DO NOT hold the transmit (PTT) switch on when not actually desiring to transmit.

DO NOT allow children to play with any radio equipment containing a transmitter.

DO NOT operate a transmitter near unshielded electrical blasting caps or in an explosive atmosphere unless it is a type especially qualified for such use.

COMPUTER SOFTWARE COPYRIGHTS

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MOTOROLA

INSTRUCTION MANUAL REVISION

FMR-886
Issue 4

for

Manual No. 68P81014C65-A
RDX1000 Portable RF Data
Terminals 403-430, 440-512 MHz
Models N1257A, N1258A

GENERAL

This revision outlines changes that have occurred since the printing of your instruction manual. Use this information to supplement your manual. Installation of these changes in earlier equipment is not necessary except as recommended in Motorola Service and Repair Notes (SRN's).

REVISION DETAILS

(N/C = no change in suffix)

No.	Change Affects	Item Number	Suffix
1	Schematic Diagram, Circuit Board	NLN4992A	1
	Detail, and Parts List	NLN7219A	1
2	Schematic Diagram, Circuit Board	NLN4995A	5
	Detail, and Parts List	NLN7218A	1
3	General Information	----------	N/C
4	The attached Appendix B describes a two-of-five bar code date encoding scheme developed for the terminal's light pen.	----------	N/C
5	Schematic Diagram, Circuit Board	NLN4995A	6
	Detail, and Parts List	NLN4992A	2
		NLN7219A	2
6	Parts List	NLN5390A	1
7	Parts List	NLN5389A	1
8	General Information	---	--

CHANGES

No.	Ref. Sym.	Action	Part Number	Description
1	C905	changed to	2182358G29	CAPACITOR, Fixed: 125 pF ±5%; 100 V
	R919/ 923	added	0600185A73	RESISTOR, Fixed: 10 k ±5%; 1/8 W (located from pin 16, U903 and C905. Cut pin 16, U903 and 1-and between C905 and pin 4, U903).
	U905	changed to	5105461G05	INTEGRATED CIRCUIT: CMOS; Gate type MC14023 BCP
2	C817/ 821	added	2182358G95	CAPACITOR, Fixed: 30 pF ±10%; 75 V (located on solder side from U811, pin 2 to ground).

3 Add the following "Back-Dating Information" to your manual.

BACK-DATING INFORMATION

KIT AND SUFFIX NO.	REFERENCE SYMBOL	CHANGE
NLN4992A-1		As shown
NLN4995A-1	C801	Was 2382397D09, 6.8 uF
		Added jumper wires between pins 3 and 14 of U811 and pins 10 and 15 of U810
NLN4995A-2	C801	Changed to 2382397D04, 15 uF
NLN4995A-3	C804	Was 2184008H13, .05 uF
		REVISED CIRCUIT BOARD
NLN4995A-4	C816	Added
NLN4995A-5		As shown
NLN7218A-1		As shown
NLN7219A-1		As shown

4 Appendix B (See attached pages 3 & 4).

Item No.	Ref. Sym.	Action	Part Number	Description
5	C818/ 822	added	2182358G95	CAPACITOR, Fixed: 30 pF ±10%; 75 V (located on solder side from U807, pin 2 to pin 3)

APPENDIX B

1. INTRODUCTION

The purpose of this section is to define the two-of-five (2/5) bar code and to provide a guide for the production of the bar code media. This reference is intended only as a guide, since media quality depends upon the discretion of the ultimate user.

2. MEDIA

a. Contrast Ratio

The contrast ratio of the media depends on the reflectance of the paper (white background) and the density of the print (black bars). Contrast, expressed in terms of the print contrast ratio (PCR), is defined by the following formula:

$$PCR = \frac{\text{Reflectance of Paper} - \text{Reflectance of Bars}}{\text{Reflectance of Paper}}$$

Reflectance must be measured with respect to the light source to be used to read the bar code. In most cases, code 2/5 will be printed with carbon-based ink, and an infra-red light source used in the pen. Therefore, the reflectometer used to measure the reflectance should use an infra-red filter. A minimum PCR of 0.8 will ensure satisfactory results.

b. Size

Scan rate is to a degree a function of the physical size of the media being scanned. The full 3 to 30 in./sec. scan rate range is applicable for the 2/5 code as long as the narrowest element (bar or space) is no narrower than 0.010 inches, and the widest element is no wider than 0.110 inches. If the media elements vary outside of these limits, decoding accuracy for data collected at the extremes of the scan rate range (either 3 in./sec. or 30 in./sec.) will degrade. For example, media whose narrowest element is 0.0075 inches (the highest density which can be accurately read with an 0.008 inch (aperture light pen) suffers from decreased decoding accuracy when the scan speed exceeds 25 in./sec. This results in lower than normal data read rates during very high speed scans. Conversely, media whose widest element is 0.2 inches will not be readable at scan speeds less than 5 in./sec.

Normal, comfortable scan speeds, although subject to individual technique, are usually in the range of 4 in./sec. to 25 in./sec. Long code strings (many characters in the code line) tend to inadvertently cause the operator to accelerate (double or triple) the scan speed near the end of the scan.

c. Two-of-Five Code Structure (See Figure B1)

This code provides a set of 10 unique combinations (characters) based on five bits for each character. Two of the five bits (wide elements) are binary ones and the remainder (narrow elements) are zeros. These 10 combinations are assigned to the ASCII characters 0 thru 9 (see Table B1). Character strings can vary from a minimum length of one character to a maximum length of 32 characters.

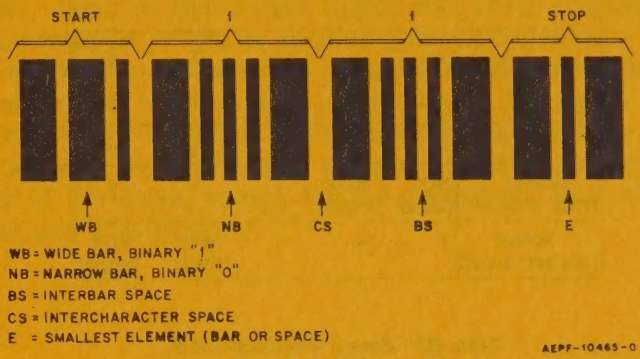

Figure B1. Code 25 Data Field

The Start and Stop characters are obtained via an abbreviated three bar field that provides positive recognition of the beginning and end of the data string. Note that only bits b_3 thru b_5 are used for the Start character and bits b_1 thru b_3 are used for the Stop character.

Keyboard control functions (BRT, DIM, ENT, etc.) can be initiated from the light pen by scanning specially printed data fields encoded as four-of-five. This scheme produces five characters that contain 4 binary ones (wide elements) and one binary zero (narrow element). Therefore, by combining two four-of-five encoded characters, sixteen control codes and nine punctuation marks are produced (see Table B3 and B4).

When producing bar codes, wide elements should be no less than two, but no more than three times the width of the narrow bar code elements. Intercharacter spacing is not constrained by the definition of code 2-of-5, and therefore may vary within reasonable limits. The intercharacter spaces should be no narrower than the narrowest element (E), and no wider than .110 inches, in order to preserve the full scan rate range.

d. Two-of-Five Encoding Data (See Tables B1 and B2)

The following tables present the bit pattern for the 10 characters recognized by this encoding scheme. These tables are included as an aid in the production of bar code labels.

Table B1. Binary 2/5 Code Table

	b_1	b_2	b_3	b_4	b_5
1	1	0	0	0	1
2	0	1	0	0	1
3	1	1	0	0	0
4	0	0	1	0	1
5	1	0	1	0	0
6	0	1	1	0	0
7	0	0	0	1	1
8	1	0	0	1	0
9	0	1	0	1	0
0	0	0	1	1	0
START (LEFT SIDE)	NOT USED	NOT USED	1	1	0
STOP (RIGHT SIDE)	1	0	1	NOT USED	NOT USED

Table B2. Binary 4/5 Code Table

	b_1	b_2	b_3	b_4	b_5
A	0	1	1	1	1
B	1	0	1	1	1
C	1	1	0	1	1
D	1	1	1	0	1
E	1	1	1	1	0

NOTE

The use of A thru E to represent the 4-of-5 encoded characters is for reference only. These bar/space patterns cannot be used to enter the alpha characters A thru E into the terminal memory.

Table B3. Control Code Symbol Assignments

FUNCTION	CODE 2/5 SYMBOLS (SEE TABLE B2)
INSERT (INS)	AA
ON (ON)	AB
BRIGHT (BRT)	AC
DIM (DIM)	AD
DELETE (DEL)	BA
CLEAR MEMORY (CL-M)	BB
PROGRAM ATTENTION (PA) SEE NOTE 2	BC
CLEAR INPUT (CL-I)	BD
BACKSPACE (←)	CA
TAB RIGHT (→|)	CB
ENTER (ENT)	CC
TAB LEFT (|←)	CD
FORWARD SPACE (→)	DA
CLEAR TO END-OF-FIELD (CL-F)	DB
PROGRAM FUNCTION (PF) SEE NOTE 2	DC
RESET (RES)	DD

Table B4. Punctuation Mark Symbol Assignments

CHARACTER ENTERED TO DISPLAY	CODE 2/5 SYMBOLS (SEE TABLE B2)
,	AE
*	BE
–	CE
$	DE
?	EE
SPACE	EA
.	EB
/	EC
=	ED

NOTES:

1. Table entries contained within ( ) correspond to keypad labels.

2. The individual PA and PF functions (PA A thru C and PF A thru L) are normally accessed via the keypad by striking either the PA or PF key followed by the desired alpha character key. (This method has not changed and is still available for operator use.) Because it is also desirable to access the PA/PF functions via the light pen, and since the 2/5 character set does not contain alpha characters, the following scheme has been devised. Enter the PA or PF mode using either the light pen or the keyboard. The terminal is now ready to accept either an alpha input from the keyboard only or a numeric input from the light pen only. (Alpha data from the keyboard is processed in the normal manner.) Numeric data (in the PA/PF mode only) is decoded at the terminal into the appropriate PA/PF function. Decoding occurs per the following:

PA 1 thru PA 3 corresponds to PA A thru PA C respectively.

PF 1 thru PF 9, and PF 0 corresponds to PF A thru PF J respectively.

PF K and PF L are accessed via the keyboard only.

Note that the use of 0 thru 9 to represent alpha characters is restricted for use with the PA/PF functions only, and cannot be used to enter alpha data into the terminal memory via the light pen.

The RDX1000 Code 2-of-5 Control Card (Motorola No. 68P81023C40) contains selected control codes and numeric data suitable for most applications. It is provided for user convenience.

(cont'd) CHANGES

No.	Ref. Sym.	Action	Part Number	Description
				DIODE:
6	CR1003	changed to	4805824C01	Silicon
7	CR1001,1002	changed to	4805824C01	Silicon

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MOTOROLA

RDX 1000

Portable RF Data Terminals

403-430, 440-512 MHz

MODELS N1257A, N1258A

CONTENTS

SECTION	PAGE
Foreword	inside front cover
List of Illustrations	ii
Specifications	iii
Model Chart	iv
DESCRIPTION	
1. Introduction	1
2. Model Variations and Options	1
3. Physical Description	2
4. Rechargeable Batteries	3
BATTERY REPLACEMENT	4
BATTERY CHARGING	
1. Chargers	5
2. Batteries	5
3. Characteristics	5
4. Maintenance	6
5. Storage	6
6. Warranty	6
THEORY OF OPERATION	
1. Introduction	7
2. Basic Functional Description	7
3. Detailed Circuit Description	12
DISASSEMBLY PROCEDURES	
1. General	33
2. Removing And Separating The Front Cover Assembly	33
3. Removing And Separating The Processor And Interface Boards	33
4. Removing And Separating Radio Section From Terminal	33
5. Servicing The Radio Modules	33
6. Removing The Radio Circuit Board From The Radio Frame	33
7. Removing The Control Flex Circuit	34
8. Removing The Power Flex Circuit	34
TEST EQUIPMENT AND SERVICE AIDS	
1. General	36
2. Test Equipment	36
3. Special Service Aids	36
4. ST1175 Dummy Battery Block	36
5. SKN6028 Or NKN6222 Tune-Up Cable	37
6. S1349A Portable Test Set	37
RADIO ALIGNMENT PROCEDURES	
1. General	38
2. Receiver Alignment	38
3. Transmitter Alignment	39
TROUBLESHOOTING	
1. General	39
2. Radio Service Notes	39
3. Radio Module Removal Instructions	40
4. Accessory Connector	40
5. Radio Performance Checks Using The S1349A Portable Test Set	41
6. Radio Receiver Troubleshooting	41
7. Radio Transmitter Troubleshooting	43
8. Data Terminal Troubleshooting	45
REPAIR, PARTS ORDERING, AND REPLACEMENT	
1. MOS Circuit Handling Precautions	59
2. Radio Circuit Board Repair	59
3. Flexible Circuit Repair	59
4. Replacing The Top Escutcheon	60
5. Replacing Controls	61
Schematic Diagrams, Component Layout Diagrams, and Parts Lists	62
APPENDIX A	A-1
Replacement Parts Ordering	inside back cover

LIST OF ILLUSTRATIONS

FIGURE		PAGE
1	Data Terminal Outline	2
2	General Block Diagram, Overall Data Terminal	7
3	Block Diagram, Radio Circuits	8
4	Block Diagram, Data Terminal Interface and Processor Circuit Boards	9
5	ID Code Formats	10
6	ID Code Bit Stream	11
7	Simplified Light Pen System	12
8	Typical Crystal Filter Response Curve	13
9	Discriminator Simplified Waveforms	14
10	Receiver Channel Element; CE1, CE2	15
11	Transmitter Offset Channel Element; CE101, CE102	15
12	Regulator/Interface Module U811	18
13	Block Diagram, Keyboard/Display Circuits	20
14	Timing Diagram, Differential Phase Shift Keying	22
15	Word Select Signal	22
16	Code Plug Control Signals	23
17	Timing Diagram, ID/Sync Decoder	24
18	Overall Timing Diagram, Processor Board	28
19	Light Pen Block Diagram	29
20	Light Pen Interface Circuitry	30
21	Simplified Data Capture Flowchart	32
22	Disassembly Drawing	35
23	Radio Module Locations	40
24	Accessory Connector Troubleshooting Diagram	41
25	Preselector Circuits, Troubleshooting Diagram	41
26	Squelch Circuit Troubleshooting Diagram	43
27	PLL Troubleshooting Diagram	44
28	General Overall Troubleshooting Flow Chart	47
29	Interface Board Troubleshooting Flow Chart (Part 1)	48
30	Interface Board Troubleshooting Flow Chart (Part 2)	49
31	Processor Board Troubleshooting Flow Chart (Part 1)	51
32	Processor Board Troubleshooting Flow Chart (Part 2)	52
33	General Troubleshooting Flow Chart, Light Pen	53
34	Light Pen Circuit Photos	56
35	Light Pen Interface Board Troubleshooting Flow Chart (Part 1)	57
36	Light Pen Interface Board Troubleshooting Flow Chart (Part 2)	58
37	Light Pen Interface Board Troubleshooting Flow Chart (Part 3)	58
38	Typical Four-Layer Board Construction	59
39	NLN4995A Data Terminal Interface Board Schematic Diagram	62
40	NLN4995A Data Terminal Interface Board Component Layout Diagram and Parts List	63
41	NLN4992A Data Terminal Processor Board Schematic Diagram	64
42	NLN4992A Data Terminal Processor Board Component Layout Diagram and Parts List	65
43	NLN7218A Data Terminal Interface Board w/Light Pen Circuitry Schematic Diagram	66
44	NLN7218A Data Terminal Interface Board w/Light Pen Circuitry Component Layout Diagram and Parts Lists	67
45	NLN7219A Data Terminal Processor Board w/Light Pen Circuitry Schematic Diagram	68
46	NLN7219A Data Terminal Processor Board w/Light Pen Circuitry Component Layout Diagram and Parts Lists	69
47	Radio Section, Control Flexible Circuit (NLN4171B)	70
48	Radio/Terminal Interface, Interconnect Flexible Circuit (NLN5391A)	70
49	Light Pen Connector (NKN6259A)	70
50	Radio Section, Schematic Diagram	71
51	Radio Section, Main Circuit Board Component Layout Diagram and Parts List	72
A1	Code 39 Data Field	A-1

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Portable Products Division
8000 W. Sunrise Blvd., Ft. Lauderdale, FL 33322
Printed in U.S.A. 7/80

SPECIFICATIONS

	RADIO TRANSMITTER
Frequency Range	403 - 430 and 440 - 512 MHz
RF Power Output	2 W
Modulation Type	15F2
Frequency Stability	0.0005% (-30° C to +60° C; +25° C reference)
Frequency Spacing	6 MHz (no degradation)
Output Impedance	50 ohms
Spurious and Harmonic Frequencies	-59 dB
FM Noise	-60 dB
	RADIO RECEIVER
Frequency Range	403 - 430 and 440 - 512 MHz
Frequency Stability	0.0005% (-30° C to +60° C; +25° C reference)
Sensitivity	0.35 uV (12 dB SINAD)
Selectivity	85 dB (EIA SINAD)
Spurious and Image Signal Rejection	80 dB
Intermodulation	75 dB (EIA SINAD)
Channel Spacing	25 kHz
	DATA TERMINAL
Keyboard	53 keys, eight with dual functions
Display	16 characters; each one comprising a 14-segment LED (plus decimal point) 0.135 in. high by 0.080 in. wide
Data Modulation Type	Audio differential phase shift keying
Data Subcarrier Frequency	1200 Hz
Data Transmission Rate	80 characters/sec (1200 bits/sec)
Signalling Reliability	Meets EIA Specification RS 374A*
Data Storage Size	480 characters
Message Error Protection	Message block check, bit error detection, and forward error correction
Weight	Complete data terminal (with radio transceiver) 29.5 oz. (Battery weight excluded)
	BATTERY
Capacity	** 8 hours; based on duty cycle of 2% receive, 2% transmit, 25% compose/read, and 71% standby
Size and Weight	Height / Width / Depth / Weight
** High Capacity	3.55 in. / 2.73 in. / 1.41 in. / 14.0 oz.
Medium Capacity	1.83 in. / 2.73 in. / 1.41 in. / 7.3 oz.
	LIGHT PEN (BAR CODE READER)
Resolution	0.0075 in. bars and spaces, 9.4 characters/in. maximum
Reading Angle	Wand angle from vertical to 45° (optimum from 10° to 35°)
Scan Velocity	Up to 30 inches/sec with minimal attenuation
Output Signal	
In Free Air	0.33 ± 0.2 V
Typical White Paper	Free air +0.12 V minimum
Black Printed Area	Near free air signal, depending on reflectivity
Power Requirements	+5.5 V ±5% dc, 55 mA (with LED on), 4 mA (with LED off)
Physical Characteristics	
Diameter	0.5 in.
Length	7.2 in.
Cord Length	5 ft. (coiled)
Temperature Range	-30°C to +60°C (operating), -40°C to +85°C (storage)
Humidity	0 to 95% (non-condensing)
Weight	4.0 oz.

* RS 374A is a proposed EIA specification for data signalling (dated Feb. 1977)

Specifications subject to change without notice.

MODEL CHART
FOR
N1257A & N1258A PORTABLE
RF DATA TERMINALS

CODE:

[X] = ONE ITEM SUPPLIED

[A] = ALTERNATE ITEM SUPPLIED, CHOICE DEPENDS ON CARRIER FREQUENCY

[O] = ITEM OMITTED

ITEM	DESCRIPTION	MODEL: N1257A	N1258A	OPTIONS: R213AA	H108AA	H320BW	H321BM	R195AA
	DESCRIPTION: RDX1000 RF DATA TERMINAL, DATA ONLY							
	DESCRIPTION: RDX1000 RF DATA TERMINAL, DATA AND VOICE							
	DESCRIPTION: DATA DUPLEX-VOICE SIMPLEX							
	DESCRIPTION: ANTENNA SUBSTITUTION							
	DESCRIPTION: CARRYING CASE, SUBSTITUTION							
	DESCRIPTION: CARRYING CASE, OMIT							
	DESCRIPTION: LIGHT PEN (BAR CODE READER)							
NAE6222A	ANTENNA, WHIP				X			
NAE6231A	ANTENNA, HELICAL (403-430 MHz)	A	A		O			
NAE6232A	ANTENNA, HELICAL (440-470 MHz)	A	A		O			
NAE6233A	ANTENNA, HELICAL (470-512 MHz)	A	A		O			
NFE6001A	FILTER (403-440 MHz)	A	A					
NFE6002A	FILTER (440-512 MHz)	A	A					
NLN8788A	FRAME	X	X					
NHN6300A	HOUSING	X	X					
NLE6931A	PRESELECTOR (403-430 MHz)	A	A					
NLE6932A	PRESELECTOR (440-470 MHz)	A	A					
NLE6933A	PRESELECTOR (470-512 MHz)	A	A					
NLE6972A	OSCILLATOR OFFSET (26.4 MHz)	A	A					
NLE6973A	OSCILLATOR OFFSET (24.4 MHz)	A	A					
NLE6975A	OSCILLATOR OFFSET (21.4 MHz, 440/512 MHz)			X				
NLE8001A	POWER AMPLIFIER (403-440 MHz)	A	A					
NLE8002A	POWER AMPLIFIER (440-470 MHz)	A	A					
NLE8003A	POWER AMPLIFIER (470-512 MHz)	A	A					
NLE8040A	CIRCUIT BOARD (403-440 MHz)	A	A					
NLE8041A	CIRCUIT BOARD (440-470 MHz)	A	A					
NLE8042A	CIRCUIT BOARD (470-512 MHz)	A	A					
NLE8062A	ANTENNA MATCHING	X	X					
NLE8181A	POWER AMPLIFIER (403-440 MHz)	A	A					
NLE8182A	POWER AMPLIFIER (440-470 MHz)	A	A					
NLE8183A	POWER AMPLIFIER (470-512 MHz)	A	A					
NLE8342A	PLL PROCESSOR MODULE	X	X					
NLE8801A	VCO MODULE (403-430 MHz)	A	A					
NLE8802A	VCO MODULE (440-470 MHz)	A	A					
NLE8803A	VCO MODULE (470-512 MHz)	A	A					
NLN5218A	COVER, BACK	X	X					
NLN4131A	CLIP, GROUND	X	X					
NLN4171B	CONTROL FLEXIBLE CIRCUIT	X	X					
NLN4990A	NAMEPLATE	X						
NLN8822A	ESCUTCHEON & KNOB	X						
NLN4992A	PROCESSOR BOARD	X	X					O
NLN8817A	ESCUTCHEON & KNOB		X					
NLN5860A	BATTERY, HIGH CAPACITY	X	X					
NLN4995A	INTERFACE BOARD	X	X					O
NLN5003A	KEYBOARD (WITH FRONT COVER, MICROPHONE, AND SPEAKER)	X	X					
NLN5391A	INTERCONNECT FLEXIBLE CIRCUIT	X	X					
NLN4999A	CARRYING CASE, STANDARD	X	X			O	O	
NLN5000A	SHOULDER HARNESS	X	X					
NLN5002A	NAMEPLATE		X					
NLN5184A	CARRYING CASE, BELT LOOP					X		
KXN1067A	CHANNEL ELEMENT (STANDARD)	X	X					
NLN4701A	CODE PLUG	X	X					
NLN5007A	LIGHT PEN W/CABLE AND CONNECTOR							X
NKN6259A	FLAT RIBBON CABLE W/3-M CONNECTOR AND LIGHT PEN CONNECTOR							X
NLN7221A	LIGHT PEN HOLDER (FOR STANDARD CASE)							X
NLN7220A	PROM KIT (3 OF 9) CODED							X
NLN7218A	INTERFACE BOARD W/LIGHT PEN CIRCUITRY							X
NLN7219A	PROCESSOR BOARD W/LIGHT PEN CIRCUITRY							X

DESCRIPTION

1. INTRODUCTION

The RDX1000 portable RF data terminal provides the ability to store and display alphanumeric data received either from a remote terminal control unit (via a radio transmitting base station) or from its own self-contained keyboard or bar code reader. The terminal enables the user to enter, retrieve, modify, or delete data in its memory and to cause the revised memory contents to be transmitted to a central computer site (via base station and terminal control unit) for storage or additional processing.

The terminal uses the latest in microelectronic technology, including LSI integrated circuits, hybrid modules, a light-emitting diode (LED) display, and a complete alphanumeric keyboard. In the radio portion of the terminal, crystal filters and hybrid technology eliminate all i-f and discriminator tuning adjustments. Only the RF circuits require tuning in the receiver. The transmitter contains a phase-locked loop circuit to generate the carrier frequency in the UHF band without need for multiplication in the RF amplifiers. This produces a transmitter that is very simple to align.

In the data processing portion of the terminal, two printed circuit boards contain all the circuitry needed to interface with the radio, detect the binary data bit stream when receiving information (or generate a binary data bit stream when sending information), and store and process the data in accordance with the nature of the transaction. The formatting controls that govern the use of both the keyboard and the data received from the central computer are contained within a 480-character random access memory (RAM) in the terminal. A microprocessor unit interprets format controls, services the display and keyboard, and initiates/receives transmissions to and from the central site. Operating software for the terminal is stored in a read-only memory (ROM).

2. MODEL VARIATIONS AND OPTIONS

Both the Models N1257A and N1258A are designed as portable data terminals for use in industrial applications. A major feature of these terminals is their compatibility with the widely used IBM 3270 Information Display System. In this respect, they are supported by the communications software and operating systems and other communications equipment that support the different display systems.

Model N1257A is classified as a "data-only" terminal capable of transmitting and receiving data on a single RF channel in the UHF frequency range (403 to 512 MHz). Model N1258A is a "data and voice" unit capable of operating on either of two UHF channels, one for data and one for voice communications. Both models produce a radiated power output of two watts. For each installation, an RF site survey is made which consists of direct bit-error measurements to determine the location and power level of the base station for optimum coverage and minimum character miss rate.

Supplementing the basic portable terminal is a large selection of accessories. This includes different types of batteries and battery chargers, antennas, and carrying cases. Table 1 lists the various accessory items by model number.

Attachment of a hand-held bar code reader is also available as an option to the terminal. This highly-reliable, shock-resistant light pen features a LED light source which provides a high signal-to-noise ratio when reading bar codes. The codes supported by the terminal are included in Appendix A.

Table 1. List of Accessories

MODEL	DESCRIPTION
NAE6222A	Antenna, Whip (403-512 MHz)
NAE6231A	Antenna, Helical (403-430 MHz)
NAE6232A	Antenna, Helical (440-470 MHz)
NAE6233A	Antenna, Helical (470-512 MHz)
NLN8834B	Battery, Medium Capacity (1 Hour Charge Time)
NLN5860A	Battery, High Capacity (1 Hour Charge Time)
NLN4036A	Battery Charger (14 Hour), Single Unit, 220 V
NLN8856A	Battery Charger (14 Hour), Single Unit, 115 V
NLN8990A	Battery Charger (14 Hr), Multiple Unit, 115/220 V
NLN4038A	Battery Charger (1 Hour), Single Unit, 220 V
NLN8858A	Battery Charger (1 Hour), Single Unit, 115 V
NLN8988A	Battery Charger (1 Hr), Multiple Unit, 115/220 V
NLN4127A	Wall Mounting Kit (For Battery Charger)
NLN4128A	Rack Mounting Kit (For Battery Charger)
NLN4999A	Standard Carrying Case
NLN5184A	Carrying Case (With Belt Loop)
NLN7221A	Light Pen Holder (For Standard Case)

3. PHYSICAL DESCRIPTION

a. General

An overall outline of the data terminal is shown in Figure 1. Basically, the unit consists of a radio section and a keyboard/processor section. The former includes the radio receiving and transmitting circuitry, most of which is contained on one multi-layer printed circuit board. Adjacent to the radio section and mounted on the front of the unit is the complete keyboard/processor package, which consists of the keyboard and display and two double-sided pc boards. One of these boards is an interface board that includes the circuitry that receives signals from, and sends signals to, the radio section. Other functional elements on the interface board are signal processing, detection, synchronization, clock generating, and voltage regulating circuits.

The second board in the data package is the processor board which contains the data processing and memory units, including an eight-bit central processing unit (microprocessor), random access and read-only memory modules, and input/output ports that communicate with the interface board.

Each terminal contains several plug-in hybrid modules. These modules contain over 80% of the radio electronics, providing faster service and less down-time. Guide pins are provided on the modules to assist replacement and prevent incorrect insertion.

Instead of complex wiring harnesses, printed flexible circuits are used, which consist of durable plastic films and which eliminate broken, pinched, or frayed wires. All operating controls (except the PTT switch and the keyboard) are conveniently located on top of the unit. The PTT switch is covered with a weatherproof boot, permitting operation in all environmental conditions.

The terminal also has a red LED that glows when the push-to-talk switch is operated. The LED is also a battery status indicator and does not light when the battery has less than about 5 to 10% charge remaining.

The antenna input impedance is 50 ohms. This permits attaching 50-ohm cables and test equipment to the antenna jack without impedance matching adapters. This feature also permits using some accessories with any terminal, regardless of the radio frequency.

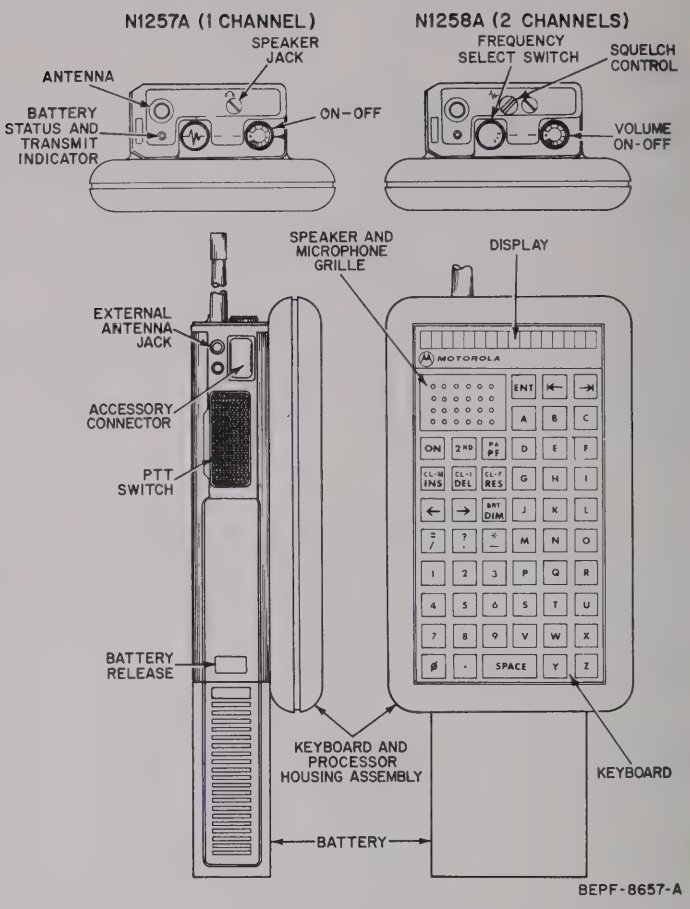


Figure 1. Data Terminal Outline

Since the battery attaches to the bottom of the unit, the terminal can operate with either of two different batteries. Batteries are available in two sizes with rapid charge rates. Refer to the battery description later in this manual. The different size batteries affect the overall height of the radio, the duty cycle, and the operating time between charges.

Every terminal has a fuse in the dc power input circuit. The fuse is on the bottom of the radio section and is replaceable without opening the radio.

The optional light pen plugs into the terminal via a five-pin connector that is accessible only when the battery is removed. Installed, the light pen connector is locked in place by the battery. This factory-installed option replaces the processor and interface boards with substitute boards that contain the light pen interface circuitry and the firmware needed to support this option.

b. Multi-Layer Circuit Board

The radio printed circuit board is a new concept in portable radio construction, involving four printed layers bonded together to form a single four-layer printed circuit board. With most of the foil pattern inside the four-layer board, less circuit is exposed to damage. Common connection points are provided where necessary on the back side of the board.

c. Control Flexible Circuit (Control Flex)

Wiring between the main radio circuit board and the controls on the frame is provided by a flexible circuit wrapped around the inside of the frame. This circuit is called the control flexible circuit, or more briefly, just "control flex."

d. Power Flexible Circuit (Power Flex)

This flexible circuit contains two high-current conductors for supplying battery voltage to the radio. The circuit attaches to the battery and fuse at the bottom of the unit and wraps around the housing to the on/off switch and ground connection at the top of the radio section.

e. Radio/Terminal Interface Cable

This 16-wire cable interfaces the data terminal portion of the RDX1000 to the radio proper and the light pen option. It also provides battery power to the terminal via direct connections to the battery.

The functions associated with each of the wires are as follows:

4 wires - provide battery power.
8 wires - provide signal and control lines between the radio and terminal.
4 wires - provide the interface connections for the light pen option.

4. RECHARGEABLE BATTERIES

The terminal is designed to operate with a 7.5-volt, rechargeable, nickel-cadmium battery. To ensure optimum capacity and performance, the battery should always be charged before using. Charging should occur, whenever possible, with the battery at about 77°F. Charging a cold battery (below 45°F) may result in leakage of electrolyte, and ultimately, in failure of the battery. Charging of a hot or warm battery (above 95°F) results in reduced discharge capacity, affecting performance of the terminal.

Motorola batteries are designed to be used with a high-quality Motorola charger. Charging in non-Motorola approved equipment may lead to permanent charger or battery damage and may void the battery warranty. The following table provides information on nickel-cadmium batteries currently available for use in the terminal. New batteries may be offered in the future; refer to your Motorola Sales Representative for latest information on batteries.

Table 2. Typical Battery Operating Hours

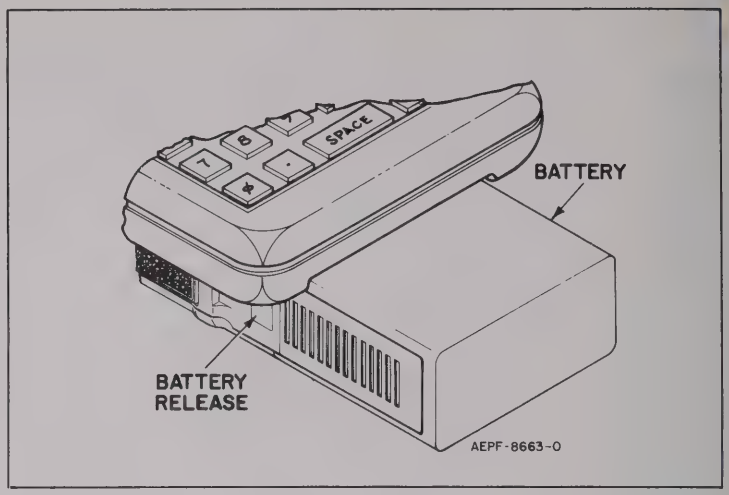
VOICE-ONLY OPERATION							
BATTERY			DUTY CYCLE (%)				HOURS OF OPERATION
MODEL	CAPACITY	MIN. CHG TIME	XMIT	RCV	COMPOSE/DISPLAY	STANDBY	
NLN8834B	Medium	1 Hour	5	5	0	90	5
NLN5860A	High	1 Hour	5	5	0	90	8
DATA-ONLY OPERATION							
NLN8834B	Medium	1 Hour	2	2	* 25	71	5
NLN5860A	High	1 Hour	2	2	* 25	71	8

* For light pen operation, the compose/display duty cycle includes a minimum 15-second display time after any individual light pen scan, or after a series of closely-timed scans.

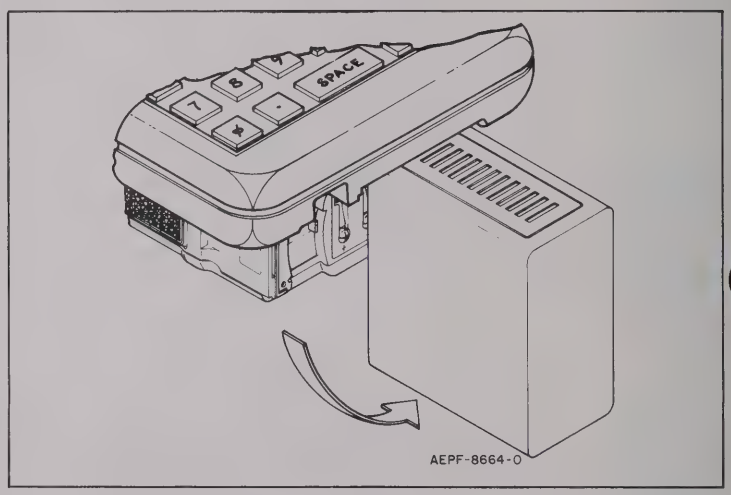
BATTERY REPLACEMENT

1. Turn the unit off.

2. Hold the unit in the left hand and press the battery release with the left thumb.

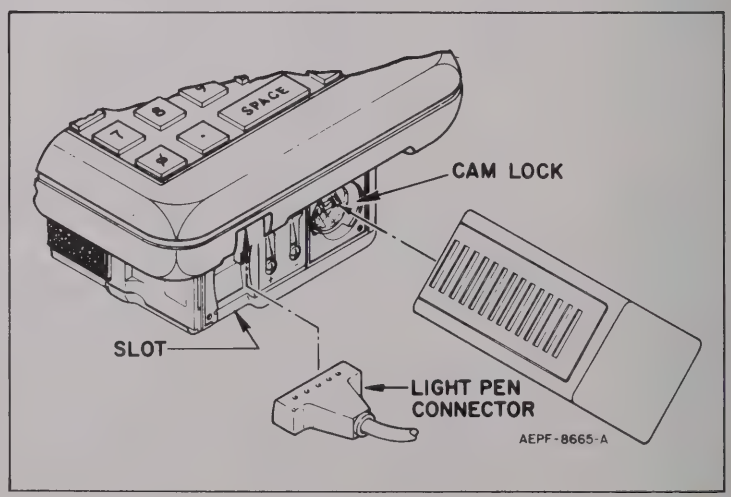


3. While holding the release depressed, rotate the battery counterclockwise as illustrated.



4. Rotate the battery about 180 degrees, until the cam lock is clear, and remove the battery from the terminal.

5. Insert the light pen connector into the receptacle as illustrated. When the battery is installed, the connector will be locked in place.



6. To replace the battery, reverse the procedure. First engage the cam lock, then rotate the battery clockwise until it latches in the proper position. Be sure the battery engages the slot on the bottom of the terminal.

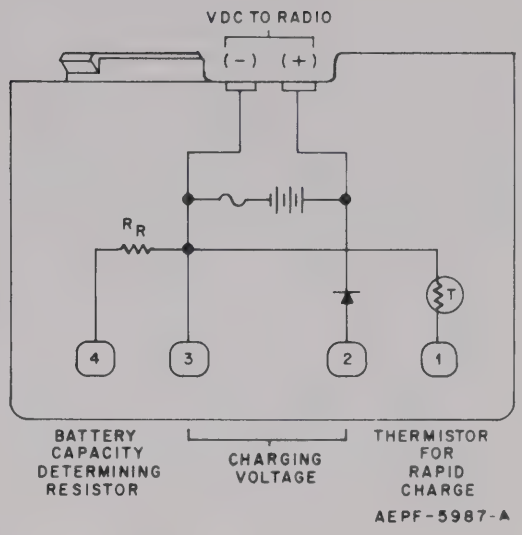
BATTERY CHARGING

1. CHARGERS

Available chargers include single-unit desk chargers and multiple-unit chargers that may be mounted on a wall or on a bench. The multiple-unit chargers will charge up to six nickel-cadmium batteries at one time.

The chargers are available in 14-hour charge and 1-hour charge models. The 14-hour chargers will charge the batteries, with or without the terminal attached, in 14 hours, while the 1-hour chargers will charge the batteries in 1 hour; see Table 3.

There are four single-unit desk chargers available. Two models operate from 115 V ac and two models operate from 230 V ac. Two multiple-unit chargers are available. These multiple-unit chargers contain a switch for selecting 115 V ac or 230 V ac operating voltage.



Typical Battery Construction, Rapid Charge, Side View

2. BATTERIES

Two batteries are available with a rapid charge rate (1 hour). They are of different sizes to provide various duty cycles and operating times, depending on operating conditions.

Charging voltage is applied to the battery through contacts in the side of the battery. The batteries have four contacts on the side. Two of the contacts receive charging voltage. The third contact connects an internal resistor (R_R) to the charger, automatically setting the charging current output to match the capacity of the battery. The fourth contact connects an internal thermistor to the charger. The thermistor senses battery temperature and automatically controls the charger output to permit maximum charger output without overheating the battery.

All rapid charge batteries contain an internal fuse for protection. A diode in the battery prevents damage from accidently shorting pins 2 and 3.

CAUTION

Sustained shorts across the radio contacts (-, +), excessive currents, or excessive heat will destroy the internal thermal fuse, which is not replaceable.

Table 3.
Charging Times for Typical Charger-Battery Combinations

BATTERY MODEL	CHARGERS	
	NLN4036A NLN8856A NLN8990A (14 hour)	NLN4038A NLN8858A NLN8988A (1 hour)
NLN8834B	14 hrs	1 hr
NLN5860A	14 hrs	1 hr

3. CHARACTERISTICS

Each nickel-cadmium battery consists of six cells connected in series to provide a nominal 7.5-volt dc output.

The voltage of a nickel-cadmium battery remains approximately constant under load until the battery approaches the discharged condition. At this time, a marked decrease in the voltage occurs and the discharged condition (1.0 V per cell) is reached abruptly. Metering to determine the state of charge in this type of battery is difficult and is not normally performed. A general characteristic of all rechargeable batteries in storage is self discharge. If the battery is used after unknown periods of storage, it is recommended that it be charged at the full charging rate, using an approved battery charger.

4. MAINTENANCE

The battery cells will never require additional electrolyte. The only maintenance required is recharging the battery and keeping the contacts clean.

Use only a Motorola approved charger. The use of other chargers, unless approved, will void the battery guarantee and may result in permanent damage to the battery. Follow the charging instructions which accompany the charger.

5. STORAGE

The battery may be stored at room temperature in any state of charge without damage. As previously stated, however, the battery is subject to self discharge and should be recharged after extended storage.

If the battery is connected to the data terminal during storage, accelerated storage discharge will occur, even if the terminal is switched off. When this mode of storage is used, recharging is recommended, if store time exceeds three days (72 hours).

6. WARRANTY

a. Service Life Warranty

Any battery failing due to defects within one year of the date stamped on the battery will be replaced without additional cost. The battery is considered defective if:

(1) It fails to meet discharge time specified in step 3 of the Battery Test Table, which reflects battery capacity.

(2) It develops apparent leakage.

b. Determining Battery Capacity by Measuring Discharge Time

Capacity for the purposes of determining liability under the provisions of this paragraph shall be determined by measuring the time that a fully charged battery requires to discharge to 6 volts through a specified load, as described in the Battery Test Table.

c. Battery Replacement

If at any time during the service period, the battery discharge time (capacity) measures less than specified in Table 4, consult your nearest Motorola Sales Representative for further instructions.

d. Limitations To Liability

The Manufacturer's Guarantee becomes VOID if:

(1) Equipment other than that approved by the manufacturer is used to charge the batteries.

(2) Charging is done at temperatures greater than 122°F without proper instructions from the manufacturer.

(3) Batteries are used in equipment or for other services for which they were not intended.

Table 4. Battery Test Table

BATTERY MODEL	STEP 1	STEP 2	STEP 3
	Discharge the battery to +6 volts through the applicable resistor listed below:	Charge the battery fully, using the applicable approved charger listed below:	Discharge the battery through the resistor listed in step 1 until the terminal voltage reaches 6 volts. Check the time required. If battery is defective, time will be less than:
NLN8834B	10.7 ohms, 10 W, 1%	NLN8858A	48 minutes
NLN5860A	6.0 ohms, 15 W, 1%	NLN8858A	48 minutes

NOTE:

1. Time measured in step 3 is measured from the time that the resistor is connected across terminals.
2. Remove the resistor load after completing step 3.

THEORY OF OPERATION

1. INTRODUCTION

This section of the manual provides a basic and a detailed functional description of the data terminal and its components. Overall functions are discussed first in general terms, with each circuit board and its relationship to other parts of the terminal described. Detailed circuit descriptions are then given for each pc board used in the equipment.

NOTE

System applications of the data terminal are not considered in this manual. For further information on system usage and communication with the central computer site, refer to the RDX1100 Control Unit manual (Motorola publication 68P81014C95).

2. BASIC FUNCTIONAL DESCRIPTION

a. Overall Data Terminal

A general block diagram of the overall data terminal is given in Figure 2. The radio portion of the terminal operates in the conventional FM two-way radio (transceiver) configuration, in which a common antenna is connected to both the receiver circuits and the transmitting circuits via a push-to-talk (PTT) relay. In the data-only models, the PTT relay is operated automatically under control of the processor in the data terminal section of the unit. For data-and-voice models, the PTT relay may also be operated manually under control of the PTT switch on the side of the unit.

The PTT relay is normally de-energized so that transmissions from the base station are received by the terminal whenever a polling or message sequence is initiated by the information display system. Each portable terminal in a network has a unique ID code assigned to it which enables it to be selectively called. If a response or an acknowledgement is required by the terminal, circuits on the processor board will generate an appropriate binary serial data output and energize the PTT relay so that the data will be transmitted back to the base station.

The data terminal itself may initiate a transmission by keying in data on the keyboard, or by reading bar coded data via the optional light pen. As a message is composed or modified, the information is stored in the terminal memory and echoed in the rightmost positions of the 16-character display. A special key (ENT) is normally depressed to cause the data to be transmitted back to the base station.

For data-and-voice models, the operator may initiate a voice transmission by operating the PTT switch and speaking into the microphone on the front of the unit. Two-channel terminals must be used for this mode of operation in which

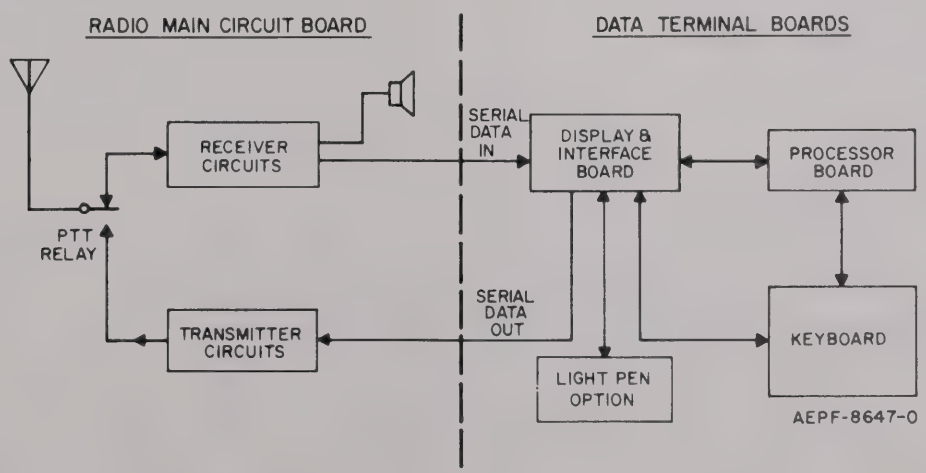


Figure 2. General Block Diagram, Overall Data Terminal

the second RF channel is reserved for the voice transmission. The RF circuits in the radio can be tuned to operate anywhere in the UHF frequency ranges of 403 to 430 MHz and 440 to 512 MHz. The transmitted FM signal is in accordance with FCC type 15F2 modulation characteristics.

b. Radio Receiver and Transmitter

Refer to the general block diagram of the radio in Figure 3. The received signal at the antenna is connected through the normally-closed PTT relay contact to the UHF preselector module (A1). This module contains filters, an RF amplifier, multiplier, and mixer circuits. The multiplier receives an input from the channel element (local oscillator), doubles the third harmonic of this signal, and produces an output at six times the RF carrier frequency. This signal is then mixed with the amplified RF input to produce the i-f frequency at 21.4 MHz. Two four-pole crystal filters and the first and second i-f amplifiers provide excellent gain and selectivity for the receiver. From the i-f stages, the signal is fed to the discriminator module (U6), which detects the audio (baseband) modulation in the FM signal. Module U7 contains a high-pass filter followed by an amplifier and low-pass filter which produces the desired audio response characteristic.

The amplified audio output from U7 is applied across the volume control and then to the output power amplifier (U8) which drives the speaker. In the data-and-voice model (N1258A), squelch module U9 receives an input from U6 (via the squelch control) and acts to squelch or unsquelch the audio amplifier circuits in U7 and U8 in accordance with the level of the signal present at the output of U6.

The transmitter circuits are activated when the PTT relay is energized, either manually by depressing the PTT switch or automatically by a signal from the data terminal circuits. Audio signals from the microphone (Model N1258A only), or binary data signals from the data terminal circuits, are coupled to the Instantaneous Deviation Control (IDC) module (U101) which shapes, filters, and limits these signals. A portion of the information signal is then applied to the transmitter channel element to control the deviation of the RF signal.

Modulation of the RF signal occurs in the channel element which contains a crystal-controlled oscillator, varactor modulators, and an output buffer amplifier. Model N1258A (data-and-voice terminal) has two channel elements, one of which is selected by a frequency selector switch on the top of the unit, depending on whether data or voice communications is being implemented.

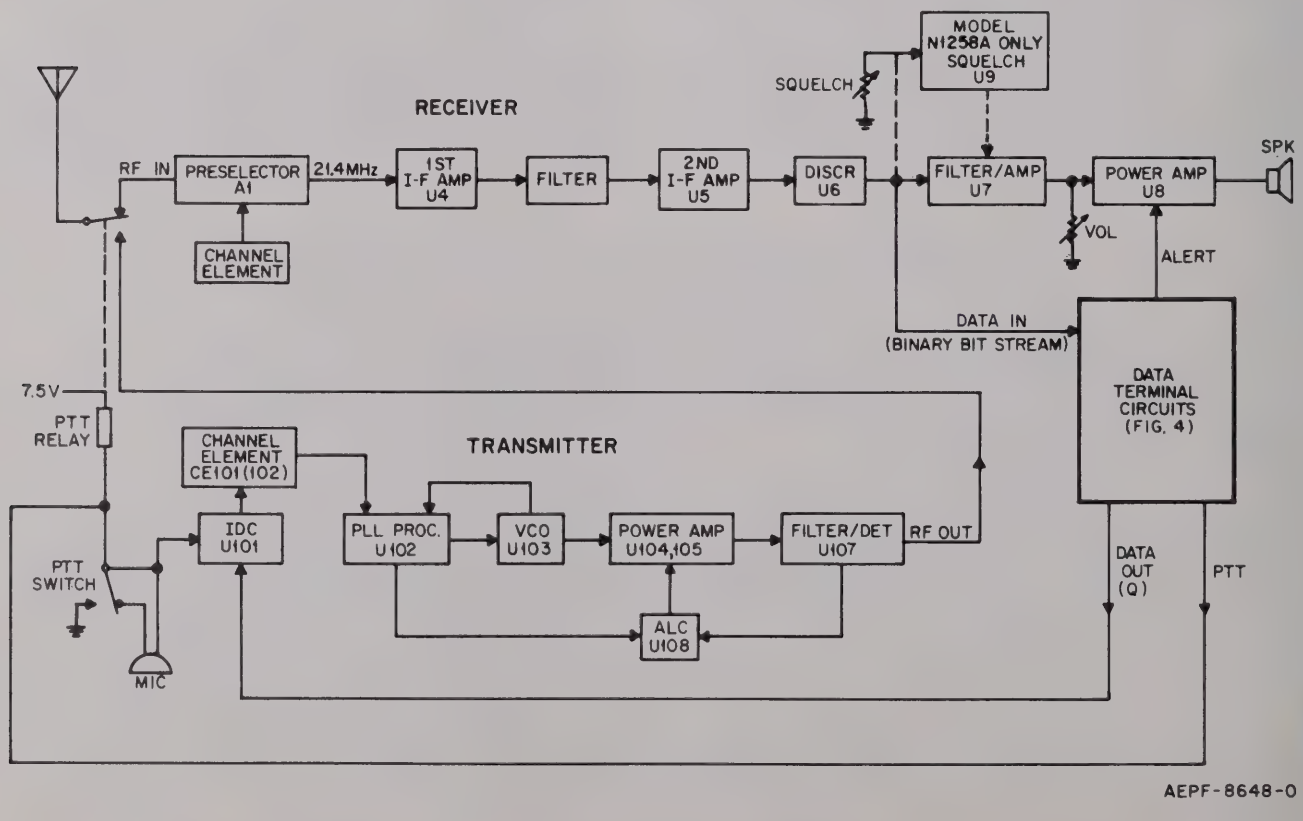


Figure 3. Block Diagram, Radio Circuits

Circuits contained on modules U102 (phase-lock-loop (PLL) processor) and U103 (voltage-controlled oscillator (VCO)) generate the transmitter carrier frequency, which is controlled by the reference frequency from the channel elements. The VCO constantly sweeps across the UHF band, and when it reaches the same frequency as that of the channel element output, the PLL locks on and stops the VCO sweep. An automatic level control (ALC) circuit in U108 is turned on by an output from the PLL module which, in turn, allows the VCO output from U103 to be amplified by RF amplifiers in U104 and U105. Harmonic signals are filtered out in module U107 and the RF output is applied to the antenna via closed contacts of the energized PTT relay. A portion of the RF output is rectified in U107 and applied to ALC module U108. This voltage is compared with a reference voltage from U102 to produce a dc control voltage which is applied to the power amplifier. Since the control voltage depends on the RF output, it maintains the power output level to a preset value.

c. Data Terminal Interface Circuits

The data terminal interface circuits are contained on one pc board which provides the interconnections and signal handling between the radio circuits and the other circuits in the data terminal (those on the processor board and the keyboard); see Figure 4. A voltage regulator is contained on module U811 which provides a regulated output at +5.5 V for distribution throughout the data terminal circuits. This is the principal logic level used in all the data processing circuits to signify a logic high (binary 1) level. (Ground level or zero volts is defined as the logic low (binary 0) level). Module U811 contains a comparator circuit that continually checks for a low battery condition from the 7.5 V battery. If such a condition is detected, a signal is generated that activates a flag line input to the microprocessor, resulting in the actual words "LOW BATTERY" appearing on the display.

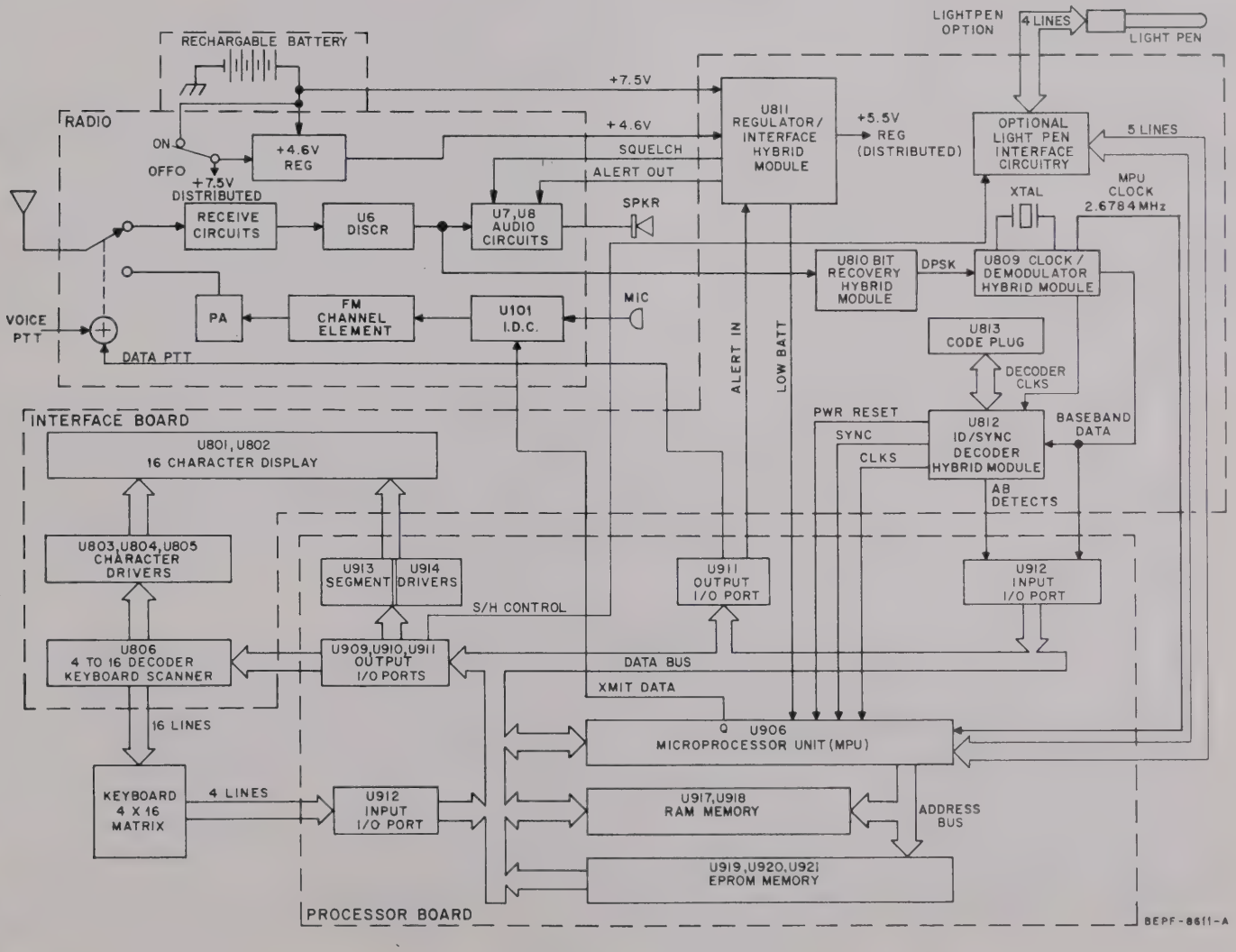


Figure 4. Block Diagram, Data Terminal Interface and Processor Circuit Boards

Marginal battery conditions produce the "LOW BATTERY" message on the display, which can be cleared by actuating either of the TAB keys (⇤, ⇥). Severely discharged batteries also produce the "LOW BATTERY" message; however, the display will flicker and cannot be cleared. Turn the unit off and replace or recharge the battery.

Clock generating circuits are all contained on module U809. A crystal-controlled oscillator provides the main clock source at 5.3568 MHz. From this frequency, three different clock rates are derived; the processor clock (2.6784 MHz), the ID/sync decoder module clock (223.2 kHz), and the demodulator circuit clock (111.6 kHz).

The keyboard comprises a 53-key input touch unit for manual entry of data. It is a 4-by-16 matrix which produces an activating input to the processor board whenever a key is depressed. Under software control, the processor then generates signals which control the 16-character LED display on the front of the unit. Character positioning, movement, and brightness level are all under program control.

The subcarrier output from the discriminator circuit (U6) of the radio receiver (which contains the audio data signal in the form of a binary bit stream) is fed to the bit recovery module (U810) on the interface board. This module consists of filtering, tracking, and shaping circuits which increase the signal-to-noise ratio of the incoming signal, optimize the symmetry of the signal, and provide logic level inputs to the demodulator circuits in module U809.

Differential phase shift keying (DPSK) is used as the modulating technique for transmitting the data to the terminal. For demodulating the DPSK signal, the recovered data bit signal from U810 is delayed precisely one bit time and then exclusive-ORed with the current data bit. This is performed by circuits on module U809. Successive bits in the data stream are thereby compared for phase relationship to recover the original base-band signal. Further details on DPSK are given in the detailed circuit descriptions that follow.

The demodulated output from U809 is used as the input to the ID/sync decoder module (U812). The circuits on this module detect the particular ID code assigned to the data terminal, as determined by the associated code plug (U813). The code plug information is continually loaded into the decoder and checked for correspondence with the input data stream. When a complete match is found, a synchronized interrupt signal is generated and sent to the processor board.

The binary ID code consists of two 23-bit "words" at 600 bits per second (bps), preceded by a 28-bit "comma" at 1200 bps. Each word contains 12 bits that make up the ID code and 11 parity bits (bits used as checks to ensure that a valid code is received). Figure 5 illustrates the formats for both the message and polling sequences used in the system. The data terminals have decimal ID code numbers or addresses. This decimal code is converted into the serial binary data stream with precise comma and space polarities as shown in Figure 6. A new

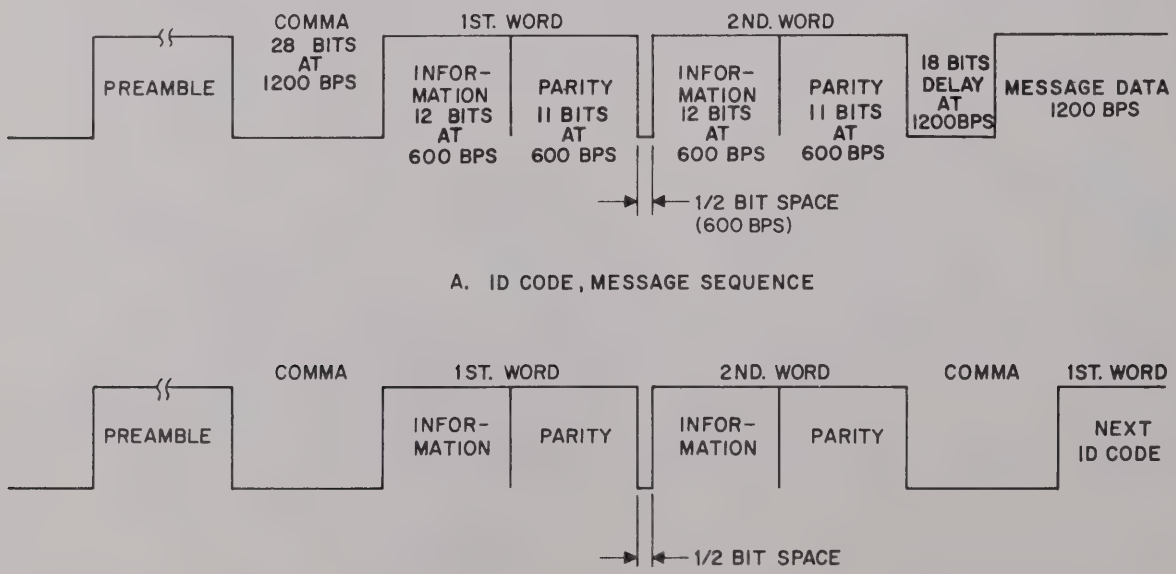


Figure 5. ID Code Formats

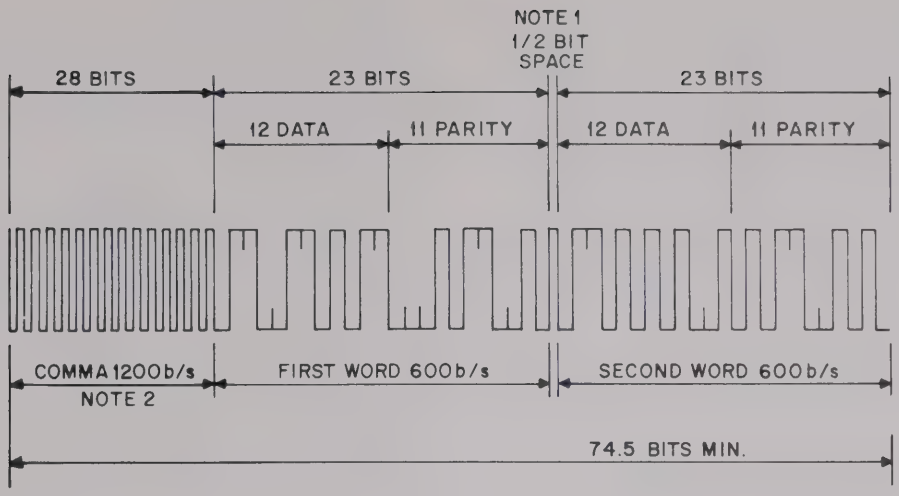


Figure 6. ID Code Bit Stream

sequence begins with the 1200-bit-per-second comma pattern which lasts for 28 bits and always precedes the first word of the ID code number. Comma polarity depends on the polarity of the first bit of the first word; i.e., the last bit of the comma must be opposite in polarity to the first bit of word 1. Preceding the ID code with comma bits prepares the decoder for the reception of the code word in such a way as to prevent detection of an ID code other than its own.

The two words that comprise the ID code are transmitted at a 600-bit-per-second rate and are separated by a 1/2 bit space, whose polarity must be opposite to that of the first bit of the second word. Using DPSK techniques, the recovered data is shifted in accordance with the 1-0 pattern of the binary code format.

Depending on the particular format of the received signal, the detection signal can represent any one of four different combinations of the words 1 and 2. These are referred to as the AB detect signals and are acted upon in the processor in accordance with system requirements, as follows:

Signal AB generated - indicates a poll for data from the control unit.

Signal $\overline{A}\overline{B}$ generated - indicates acknowledgement from control unit that terminal data was received.

Signal $A\overline{B}$ generated - indicates a poll for acknowledgement from the control unit that data was received by the terminal.

Signal $\overline{A}B$ generated - indicates a data message from the control unit.

d. Data Terminal Processor Circuits

The processor board consists of the major functional elements shown in Figure 4. The microprocessor unit (MPU) provides the overall control and central processing function for the data terminal. It is contained in a single 40-pin LSI package and features CMOS circuitry. This unit (U906) performs 8-bit parallel processing and operates at a clock rate of 2.6784 MHz. Connections to the other major units on the board are made by the 8-bit bi-directional data bus, 8-bit multiplexed address bus, and several individual control lines.

A group of five IC chips provide storage facilities for the unit. The random access memory (RAM, U917 and U918) furnishes the

working storage medium for the terminal. Operating firmware and look-up tables are stored in an erasable, programmable read-only memory (EPROM) that consists of three chips (U919, U920, and U921). These units provide the storage space for the applications program of the terminal. Addressing the modules is accomplished via the 8-bit address bus, in which five of the higher-order eight bits of an address appearing on the bus first are latched, followed by the lower-order eight bits.

Four I/O ports (three output and one input) enable parallel 8-bit data transfers to and from the interface board. These ports contain 8-bit buffer registers and are selected by individual control signals (N lines) generated by the MPU. A single mode control line determines whether a port functions in the input or output system configuration.

e. Light Pen and Interface Circuit

A block diagram of the light pen system is shown in Figure 7. The system consists of a light pen and an interface circuit (added to the interface board). Light from the pen's LED source is reflected off of the media back to a transducer that produces an analog output. At the interface circuit, the analog output is converted into digital information that is fed to the MPU for processing and display.

3. DETAILED CIRCUIT DESCRIPTION

The following paragraphs present a detailed discussion of the theory of operation for each of the circuit boards used in the terminal. These descriptions are intended to be used with the schematic diagrams in the back of the manual.

a. Hybrid Modules

The following module construction information is presented to help the serviceman better understand the terminal.

CAUTION

The hybrid modules in this terminal require very specialized equipment for repair. Do not attempt to disassemble.

The hybrid circuit modules are sealed complex circuits, consisting of both integrated circuits and discrete components. The resulting module usually performs a complete function in the terminal. The modules vary in size, depending on complexity, and have different pin configurations. The modules plug into the printed circuit boards and are easily removed for replacement.

Both thick film and thin film technologies are employed in module construction. Both types have an aluminum oxide substrate that forms the base for the circuit. The circuit paths are printed on the substrate with conductive ink in thick film modules and are vacuum deposited with metal in thin film modules.

Chip components are then reflow soldered onto the substrate. Resistors on thin film circuits are chip components, but in thick film modules, most resistors are formed by applying resistive paste between the desired points in the circuit. The paste is usually designed to provide less resistance than desired, and the resistor is trimmed later by removing excess resistive material with a laser or sandblaster, until the desired value is obtained.

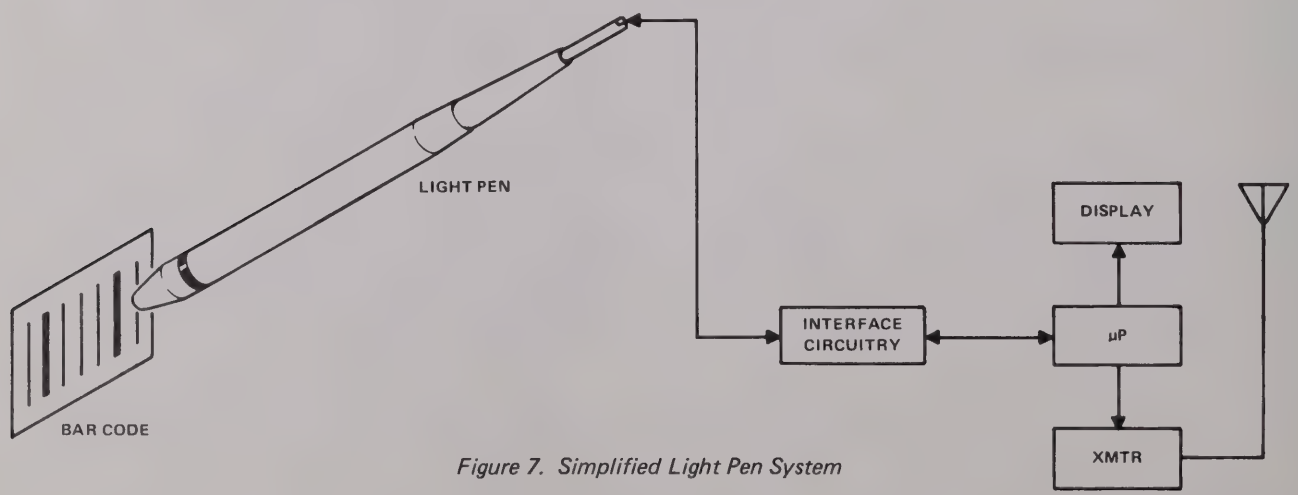


Figure 7. Simplified Light Pen System

AEPF-9980-O

Thick film capacitors are formed by printing a sandwich composed of two conductive layers separated by an insulating film. Where other capacitor values are required, chip tantalum or ceramic capacitors are attached to the circuit.

Small inductors are produced by screening spiral patterns of conductive material. When large inductors are required, discrete coils or toroids are attached to the circuit.

Active devices (transistors and integrated circuits) are bonded to the thin film substrate in chip form and connected to the circuit with hair-like gold wires. The chips are protected with epoxy. After the components are soldered in place, most of the modules are coated to keep out moisture.

b. Radio Receiver Circuits (Refer to Figure 50)

The received signal at the antenna is coupled through the antenna jack to pin 2 of relay K101. In the receive mode, with the relay de-energized, the RF signal is applied to a two-pole helical filter in the preselector. The filter output is amplified by U1 and the amplified RF signal then passes through a three-pole helical filter which provides additional selectivity. The filter output is applied to mixer U2, where it is mixed with the injection signal from multiplier U3. The multiplier receives an input consisting of multiples of (f_o) from the channel element, doubles the third harmonic of this signal, and produces a $6f_o$ output which is filtered by a two-pole helical filter and applied to the mixer. In the transmit mode, the multiplier output ($6f_o$) is also applied to the phase-lock-loop circuit in the transmitter, where it is used to develop the transmitted RF signal. Since the transmitter RF is dependent upon the receiver oscillator, the receiver circuit must be aligned before aligning the transmitter.

The received RF and the local oscillator signal are mixed in U2, producing the 21.4 MHz i-f signal, which is applied to crystal filter FL1.

The received signal from the mixer passes through crystal filters FL1 and FL2 which form a four-pole bandpass filter centered at 21.4 MHz. The overall bandwidth of the filter is about 13 kHz and the maximum insertion loss is 2 dB. A typical response curve is shown in Figure 8.

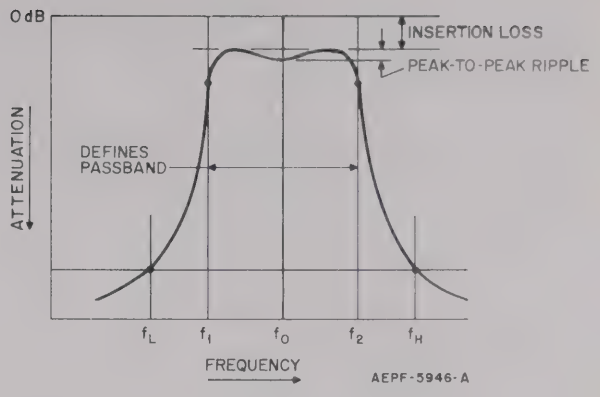


Figure 8. Typical Crystal Filter Response Curve

The filter output is applied to the first i-f amplifier U4, where the 21.4 MHz signal is amplified. This amplifier receives B+ only during the receive operating mode. The amplifier provides only gain, since selectivity and unwanted signal rejection is provided by the crystal filters.

The output of U4 is applied to crystal filters FL3 and FL4, which operate the same as FL1 and FL2, providing additional i-f bandpass selectivity. Amplifier U5 provides additional gain and also contains a limiter. Limiting occurs at low noise levels, providing a constant amplitude output at pin 8.

The amplified i-f signal from U5 is applied to a crystal discriminator (U6), incorporating 3-pole filter FL5. This crystal provides two outputs that vary in complementary fashion with the input frequency change. Detection is accomplished by applying the two signals from crystal FL5 (180 degrees out of phase) to two cascaded differential amplifiers in the module. The recovered audio appears at output pin 7. This circuit provides a high level of recovered audio output with inputs having low level deviations. Also, the circuit contains no coils and requires no adjustments.

Refer to the simplified waveforms in Figure 9. Crystal filter FL5 has two resonant circuits; 10 kHz above 21.4 MHz, and 10 kHz below 21.4 MHz. As the frequency-modulated 21.4 MHz i-f signal goes up in frequency, the crystal output amplitude at pin 2 of U6 becomes greater (point F) than the other crystal output at pin 1 of U6 (point C). These levels result in a differential amplifier output (F-C) at pin 7 as shown.

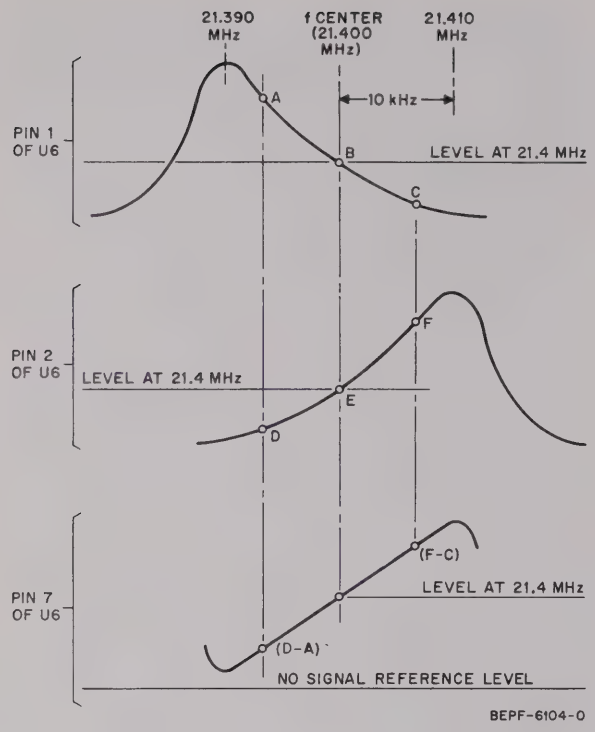


Figure 9. Discriminator Simplified Waveforms

If the signal goes down in frequency, the level at pin 1 (A) is greater than at pin 2 (D) and the resultant (D-A) at pin 7 is as shown. Total current required by the module is about 1.0 mA.

The recovered audio from U6 is applied to squelch control R311 (via C301) and to module U7. This module contains a high-pass filter circuit which attenuates frequencies below 300 Hz, preventing low frequency tones from reaching the speaker. The filtered audio output is applied to a low-pass filter and amplifier circuit in the module, which produces the desired audio response characteristic. The amplified audio output is applied across a volume control (R308) and a small series resistor (R309). The volume control forms a voltage divider and applies a portion of the audio signal to audio power amplifier module U8. The small series resistor connected to the volume control provides some audio signal to U8, even when the volume control is turned all the way down. This avoids missing voice messages by accidently having the control turned down, since a small audio output is always heard when a signal is received.

Module U7 also contains a dc voltage regulator circuit and a squelch switch circuit. The +7.5-volt battery voltage is applied to U7 during all operating modes. The regulator circuit in U7 develops +4.6 volts from the battery supply voltage and is present at pin 9 of U7 during all operating modes.

The squelch switch circuits receive inputs at pins 4, 5, and 6, and produce an output at pin 7 which squelches or unsquelches the audio amplifier circuits in module U8. If the output at pin 7 of U7 is high (+3 V), the audio circuits are squelched. If the output is low (below +0.6 V), the audio circuit is unsquelched.

If the radio is unsquelched, the low voltage at pin 4 of U8 enables the internal reference voltage. This voltage turns on the audio amplifier which produces an output across pins 1 and 9. Observe that the audio output is not referenced to ground, but is a balanced output produced by a bridge amplifier in module U8. This audio signal is applied to the speaker in the front cover via the speaker jack and the normally closed switch (S401) located in accessory connector J402. The switch is opened when a mating connector is attached to J402. This disables the internal speaker when accessories such as an external speaker-microphone are attached to the radio.

A portion of the discriminator output across squelch control R311 is applied to module U9. The signal is applied to a high-pass filter in the module and then to a limiter. The filter attenuates frequencies below about 10 kHz, removing the audio from the signal and supplying basically FM noise to the limiter. The limited noise signal is detected and applied to a logic circuit which includes external capacitor C13. When noise is present (no carrier received), the capacitor charges to a high dc voltage (about +4.5 V). When a carrier is received the voltage drops. This voltage is applied to the squelch switch circuits in U7. If the output of U9 is high (+4.5 V), the squelch switch circuit output in U7 is also high and squelches the audio amplifier in U8 by interrupting the reference voltage supply to the amplifier.

c. Channel Elements

The channel elements contain a crystal-controlled, actively compensated oscillator and a buffer output circuit. Transmitter channel elements also contain varactors for modulating the oscillator. Primary differences involve output frequency and the crystal harmonic (overtone) being used.

Refer to the simplified receiver channel element diagram (Figure 10). The crystal-controlled oscillator employs the fifth overtone of the crystal and produces an RF output to the buffer circuit. The buffer RF output (f_o) appears at pin 3. The third harmonic of the RF output is multiplied two times in the preselector to produce a $6f_o$ signal.

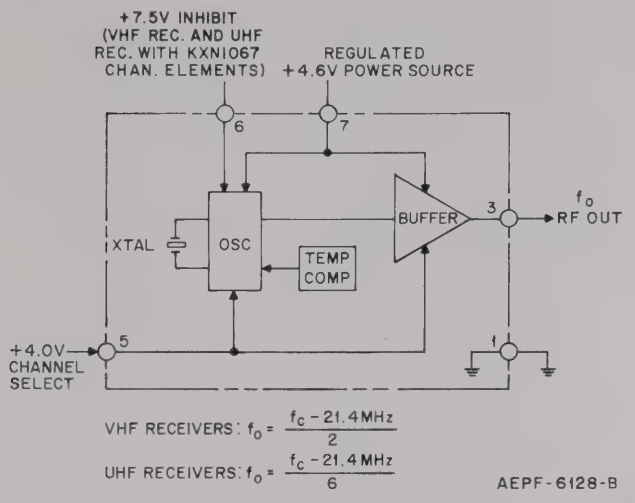


Figure 10. Receiver Channel Element; CE1, CE2

The channel element receives several dc voltages. The +4.0 V at pin 5 is supplied from a frequency selector switch (two frequency models) and enables only the selected channel element. The selected receiver channel element output must be present during transmission, since the multiplied output ($6f_o$) is used in the transmitter PLL circuit. Therefore, the +7.5 V inhibit at pin 6 is not used, except when non-standard transmitter offset is used (KXN1067 Channel Elements).

The +4.6 V at pin 7 supplies the primary power source to the channel element. The voltage is present at all receiver channel elements during all modes of operation, but only the selected one (+4.0 V at pin 5) will operate.

The transmitter carrier frequency is either the same as the receiver frequency, or 3 or 5 MHz above it (standard offset). Radios operating between 403 and 430 MHz use the 3 MHz offset, while those operating in the 440 to 470 MHz range use either the 0 or 5 MHz offset. For units operating in the 470 to 512 MHz range, the offset will normally be either 0 or 3 MHz. Other (non-standard) offsets are available.

In application, the transmitter offset channel element output supplies the modulation and the offset information to the transmitter PLL circuit. Refer to the simplified diagram (Figure 11) for the transmitter channel element. The audio input is applied to varactors in the oscillator. Also, the third overtone mode of the crystal is employed in the oscillator. Thus, audio from the IDC circuit is applied to the module at pin 2, which frequency modulates the oscillator, resulting in an FM output.

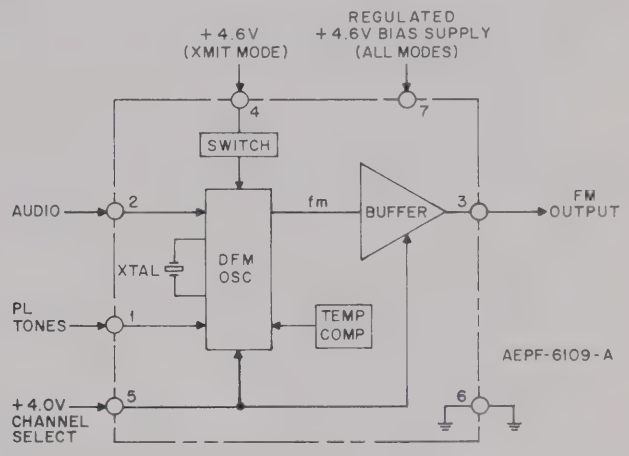


Figure 11.
Transmitter Offset Channel Element; CE101, CE102

A +4.6 bias voltage is applied to pin 7 of the transmitter channel elements in all operating modes. Terminals with two channels have a frequency selector switch that selects the desired channel element. The switch applies +4.6 V to the anode of a selected diode, which conducts and applies +4.0 V at pin 5 to enable only the selected channel element. When the PTT switch is pressed (transmit mode), +4.6 V is applied to pin 4. The dc voltage at pin 4 turns on the oscillator of the offset element enabled by the frequency selector switch.

The RF output at pin 3 is frequency modulated and has a 21.4, 24.4, or 26.4 MHz output which is then compared with the mixed frequency in the PLL module.

d. Radio Transmitter Circuits
(Refer to Figure 50)

The voltage controlled oscillator in module U103 oscillates at the RF carrier frequency. The following RF amplifiers therefore simply

amplify the VCO output, without multiplication or tuning. The transmitter alignment is also simplified by this system. The only adjustments required to align the transmitter are: (1) set the deviation, (2) warp the channel elements, and (3) set the RF power level.

Note that U105 (RF amplifier) and the class C stage of U104 have +7.5 V applied during all modes of operation. However, PLL module U102, VCO U103, and the class A stage of U104 receive B+ only during the transmit mode. B+ is removed during all other modes. Therefore, the RF amplifiers do not draw battery current when the VCO is shut down.

When the push-to-talk (PTT) switch is pressed, a ground is applied to relay K101 via terminal E1 on the main circuit board. The relay is energized and applies B+ (7.5 V dc) to modules in the transmitter at points labeled "T". Simultaneously, the relay removes B+ from the receiver circuit and switches the antenna from the receiver to the transmitter.

With the PTT switch pressed, audio at the microphone is coupled by C302 to IDC module U101, via terminal E6 on the main circuit board. The IDC module shapes, filters, and limits the audio signal. The modified audio signal is applied to deviation control R102, which applies a portion of the information to the channel elements and controls the deviation of the transmitted RF signal.

When the transmitter is keyed by the PTT switch, the PLL module (U102) generates a regulated +4.6-volt output. This voltage is applied to all channel elements and activates only the channel element selected by the frequency selector switch.

The phase-lock-loop processor and VCO circuits (modules U102 and U103) generate the transmitter carrier frequency, which will normally be the same as the receiver frequency or 5 MHz away from the receiver frequency in 403-470 MHz radios (3 MHz away in 470-512 MHz radios). This offset (Tf-Rf) is assigned by the government.

Since the transmitter frequency normally has a fixed relationship to the receiver frequency, a signal from the receiver oscillator multiplier in the preselector is used to develop the transmitter carrier frequency.

When the transmitter is first keyed, the phase/lock detector circuit in U102 generates a sawtooth sweep voltage that is filtered and applied to pin 1 of VCO module U103. This causes the VCO to sweep across the band. A sweep voltage between 1 V and 4.6 V will sweep the VCO from about 403 to 430 MHz, 440 to 470 MHz, or 470 to 512 MHz. A portion of the VCO output is applied back to a mixer circuit in U102 (pin 9). A second input to the mixer is supplied from the receiver preselector at pin 12 of U102. The $6f_o$ signal from the preselector is 21.4 MHz lower than the receiver channel frequency. These two inputs ($6f_o$ and VCO) are mixed and the difference frequency is applied to the phase/lock detector circuit, where it is phase compared with the output from the selected transmitter offset channel element (21.4, 24.4, or 26.4 MHz).

Assume that zero offset is required for the transmitter. The 21.4 MHz channel element (CE101) will be activated and the output will be applied to pin 2 of U102. When the VCO output frequency becomes equal to the receiver frequency, the mixer output in U102 will be 21.4 MHz. This mixer output is phase-compared (in the phase/lock detector) with the 21.4 MHz output from CE101 and lock occurs, shutting off the sweep voltage to the VCO. The phase/lock detector output now contains only modulation information for the VCO.

Similarly, if the transmitter frequency is offset 5 MHz, then CE102 will be activated and 26.4 MHz will be applied to pin 2 of U102. When the VCO sweeps to the desired frequency, the mixer output will be 5 MHz higher than before (26.4 MHz). This is phase compared with the signal from the offset channel element, which is also now 26.4 MHz, and lock occurs at the offset channel frequency.

When lock is achieved, U102-5 drops to a low dc voltage, allowing the automatic level control (ALC) output (U108-5) to remain high. This keeps the class A stage of U104 on. If lock does not occur within 15 ms of transmitter keying, C112 will charge to the +6 V present at U102-5 (PLL) causing the ALC output (U108-5) to go low. This action disables the class A stage of U104, inhibiting the transmitter.

The UHF international options use either the NLE8351, NLE8352, or NLE8353 modules in place of the standard VCO (U103) module. These modules include a gate circuit at the output of the VCO, as shown in Figure 27. When the trans-

mitter is keyed and the PLL is in the sweep mode, U102-5 is high (approximately +6 V) which inhibits the class A stage of U104 via ALC U108. The VCO gate is disabled by U102-7, applying a low to VCO gate U103-7.

When lock is achieved U102-5 goes low (approximately +2.3 V) causing the ALC output (U108-5) to go high, which enables the class A stage of U104. After a short time delay, U102-7 goes high enabling the VCO gate (U103) which allows the transmitter to function. If lock does not occur, U102-5 remains high and U102-7 remains low inhibiting the transmitter.

The VCO output is amplified by power amplifiers U104 and U105. The RF power amplifiers are class C amplifiers, normally biased off without an input drive signal. Amplifier U104 contains a class A amplifier driving a class C amplifier in the same module. The gain of the class A stage is controlled by varying the B+ supplied from the ALC module. If the class A stage is shut off, no drive signal is supplied to the following stages and they are also cut off.

The RF output from the last RF amplifier is applied to U107. The harmonic signals are filtered out and the RF output is applied to the antenna via closed contacts of energized relay K101.

Another circuit in U107 samples the RF signal rectifies the sample, adds it to the dc level from the power adjust control, and produces a dc output voltage at pin 2, that depends upon the RF output level and the setting of the power adjust control (R107). This dc voltage is applied to U108 where it controls the ALC circuit.

The voltage applied to U108 from U107 is compared with a reference voltage supplied from U102. The difference amplifier in U108 produces a dc control voltage at pin 5, which is a positive voltage less than +7.0 volts. This voltage level controls the gain of the class A amplifier in U104, and therefore controls the power output level of the transmitter. Since this control voltage depends upon the RF output (once the power adjust control is set) it will vary and maintain the power output level set by R107.

To understand the overall operation consider the following conditions. When the transmitter is first keyed and the VCO (U103) is not locked on frequency, the PLL module (at U102-5) supplies a high voltage (approximately +6 V) to RC network R108 and C112. Connected to the ALC input (U108-1) via R108, C112 initially holds U108-1 low, causing the output (U108-5) to go high (approximately +7 V) which enables the class A stage of U104. Because the VCO (U103) does not have a gate circuit, its output is fed directly to the input of the class A stage of U104 when the transmitter is keyed. Therefore, transmission occurs while the VCO is still in the search mode. The VCO search mode output is transmitted until the PLL locks (approximately 5 ms) or until C112 charges to a voltage that is positive enough to inhibit the ALC (approximately 15 ms). The output of the ALC (U108-5) goes low, disabling the class A stage of U104. This removes the RF drive to the filter/detector (U107), reducing the RF output to zero volts. The dc voltage at U107-2 is therefore determined only by the "power adjust" setting (R107) and is low between 0 V and +2.0 V.

When the VCO locks on frequency, the voltage at U102-5 of the PLL drops from +6 V to about 2.3 V. The dc voltage at U107-2 increases due to the rectified RF added to the dc voltage from the power adjust control (R107). The resulting higher voltage (between +2.3 V and +2.5 V) appears at U108-1 of the ALC, which reduces its output at U108-5. This output voltage will be between +7.0 V maximum (producing maximum RF power output) and about +2.0 V minimum (at the minimum power adjust setting).

e. Data Terminal Interface Board
(Refer to Figures 39 and 43)

(1) Voltage Regulator/Interface Module (U811)

When the radio on/off switch is turned on, 4.6 V from a regulator circuit in the radio (module U7) is applied as the turn-on control signal to the data terminal. The 7.5 V battery voltage is applied directly to the terminal's display drivers and to the regulator circuit on module U811, bypassing the radio on-off switch. A schematic diagram of the regulator circuits is given in Figure 12. The +4.6 V level is applied via pin 1 of U811 to switch 7.5 V to the series-pass unit in the regulator.

Regulation is provided by using the +4.6 V input from the radio circuits as a reference source to a comparator amplifier (U807A) external to U811. This voltage is also passed through a differential voltage comparator in U811 which checks for a low battery condition from the +7.5 V

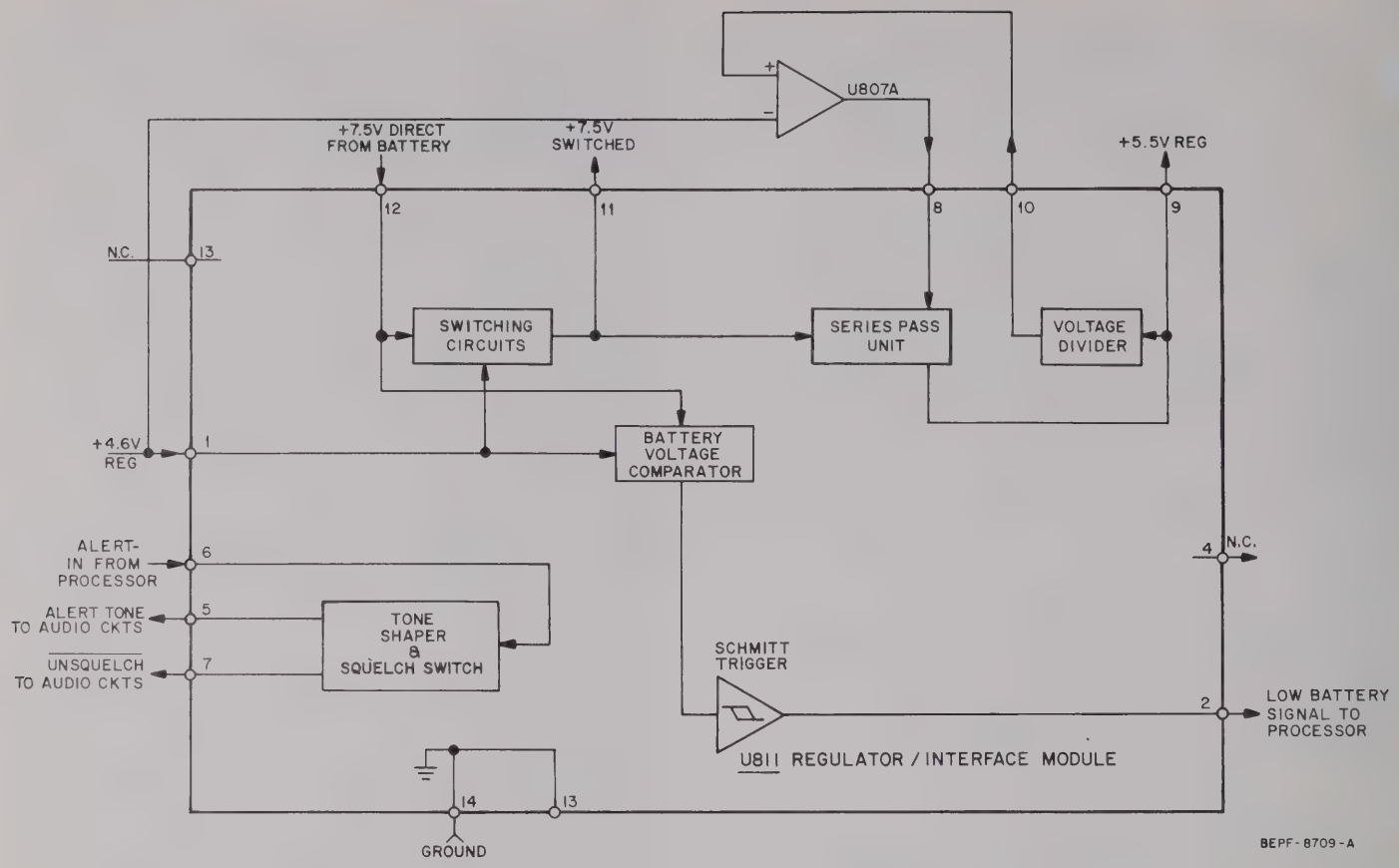


Figure 12. Regulator/Interface Module U811

battery. The battery voltage comparator circuit trickle discharges ($\simeq$ 1.5 mA) from the battery, even with the data terminal switch off. This must be considered in the recharging cycles of the battery.

If a low battery output is present, it will appear as a low logic level at pin 2 of U811. This is connected directly to the processor board as a flag input ($\overline{EF4}$) to the MPU. In effect, this inhibits the program so that no further operations take place that could result in erroneous data, because of low battery voltage.

Operational amplifier U807A functions as the regulator/comparator for the 5.5 V output. The 4.6 V from the radio is applied to the negative side of U807A, while the +5.5 V from the series-pass unit in U811 is applied to the positive side via a voltage divider at pin 10. If the + and - inputs to U807A are equal, the circuit is in equilibrium and no change occurs at the series-pass unit in the regulator. If the load on the +5.5 V output increases, the voltage tends to decrease and cause a change in the balance of U807A. This results in switching U807A to a more negative output, which in turn, causes the series-pass unit to conduct harder and thereby cause the +5.5 V output to increase.

The other circuit included in U811 is a tone shaper and squelch switch. This circuit receives the ALERT signal from the processor board and integrates it to a dc level. It then applies the level as an unsquelch control to the radio circuits, simultaneously routing the conditioned alert signal to the radio audio circuits.

Components added to the back of the radio circuit board:

Diode CR1001 is connected to +4.6 V (E17) on the one-frequency model (N1257A) to provide for squelch operation at all times other than data alert. However, in the two-frequency model (N1258A) the diode only conducts while operating on the data channel. On voice channel, the diode is switched from +4.6 V to allow proper operation of the radio carrier squelch control.

Series-connected components CR1002 and R1001 are used to minimize the modulation turn-on transient when operating in the data transmit mode. In this case, diode CR1002 conducts through the normally-closed contact of relay K101 from the +7.5 V source to R102 and ground. This action precharges the channel element input. In the transmit mode, diode CR1002 is cut off to allow normal transmit audio to pass from the IDC module (U101) to the channel element.

Jumper JU9 must always be open on the data-only model (N1257A). However, for the two-frequency, data-and-voice model (N1258A), this jumper connection must be closed to provide a path between points I9 and I10 on the radio interconnect flexible circuit. Therefore, transistor Q1001 and R1002 are added on the back of the radio board to provide for this situation; i.e., on the two-frequency model, circuit point E17 is connected to +4.6 V through the channel select switch so that Q1001 is turned on, completing the path between I9 and I10.

Jumper JU1001 is added to provide a connection for data modulation between the data terminal portion of the unit and the IDC module in the radio portion, while diode CR1003 is added to provide a connection for the channel indication between the frequency selector switch (Model N1258A only) and the data terminal.

(2) Clock Circuits (U809)

The clock source for the entire data terminal circuits is controlled by crystal Y801 connected between pins 18 and 19 of U809. This unit functions with an oscillator circuit to provide a stable frequency of 5.3568 MHz. A ripple counter in U809 then divides the clock signal by two to produce an output at pin 16 of 2.6784 MHz, which is the basic clock rate signal (CLK) applied to the MPU on the processor board. A second output from the counter is applied via pins 14 and 13 of U809 to an exclusive OR gate and flip-flop circuit to produce a signal (pin 4) at 223.2 kHz, which is the clock rate required by the ID/decoder circuits in module U812. Another divide-by-2 circuit results in a signal (pins 5 and 7) at 111.6 kHz for use in the demodulator circuits in this module (U809).

(3) Keyboard/Display Circuits

A block diagram of the keyboard/display circuits is given in Figure 13. The keyboard itself is mounted above the processor and interface boards and contains nothing but the 53 keys that comprise the input medium for manual entry of data. Even though only 53 key positions are used, the keyboard is arranged in a 4-by-16 matrix. When a key is depressed, one of the four output lines from the keyboard changes to a binary 1 while the other three lines contain binary 0's. This information is sent to the data bus via input port U912 on the processor board. At the same time under software control, a ring-type sequential counter in the MPU is continually cycling through a count from 1 to 16. This counter is interrogated at the time the keyboard input from U912 is generated. The 4-bit representative output from the counter appears on the data bus and is transferred via output port U911 to a 4-to-16 decoder. Each one of 16 lines is then activated with a positive pulse as the counter is incremented by the MPU. This action provides time correlation with the original key movement so that a particular key (character) position is identified.

The software in the processor uses the 4-bit input from U912 together with the current 4-bit counter value to form an 8-bit byte that is used as an argument against a table of values stored in the EPROM. The particular character associated with that value corresponds to the key pressed. The MPU then generates a 15-bit output via ports U909 and U910 and their associated LED driver packages. These outputs are fed directly to the 15-segment LED display elements to illuminate the appropriate character.

A brightness level control is built into the system by using the inhibit signal (INH) at pin 23 of U806. When a character is selected for display, the instantaneous current is typically 48 mA per segment. In the worst case, which is a 10-segment character, a total of 480 mA is used. However, since the duty cycle over the 16-character display scan is 1/16 of the total, the average current is about 3 mA per segment for the maximum brightness level. By applying the inhibit signal to temporarily cut off character selection, the duty cycle can be further reduced to 1/32 of the total time. This results in a dimmer display, but with a significant reduction in current drain. Also, the inhibit signal is used as a battery saver by blanking the display completely whenever no activity is present within the keyboard or output display service routines.

Since characters are displayed from right to left, character 16 is always the first one to be presented to the segment drivers whenever a new data operation is implemented. Character

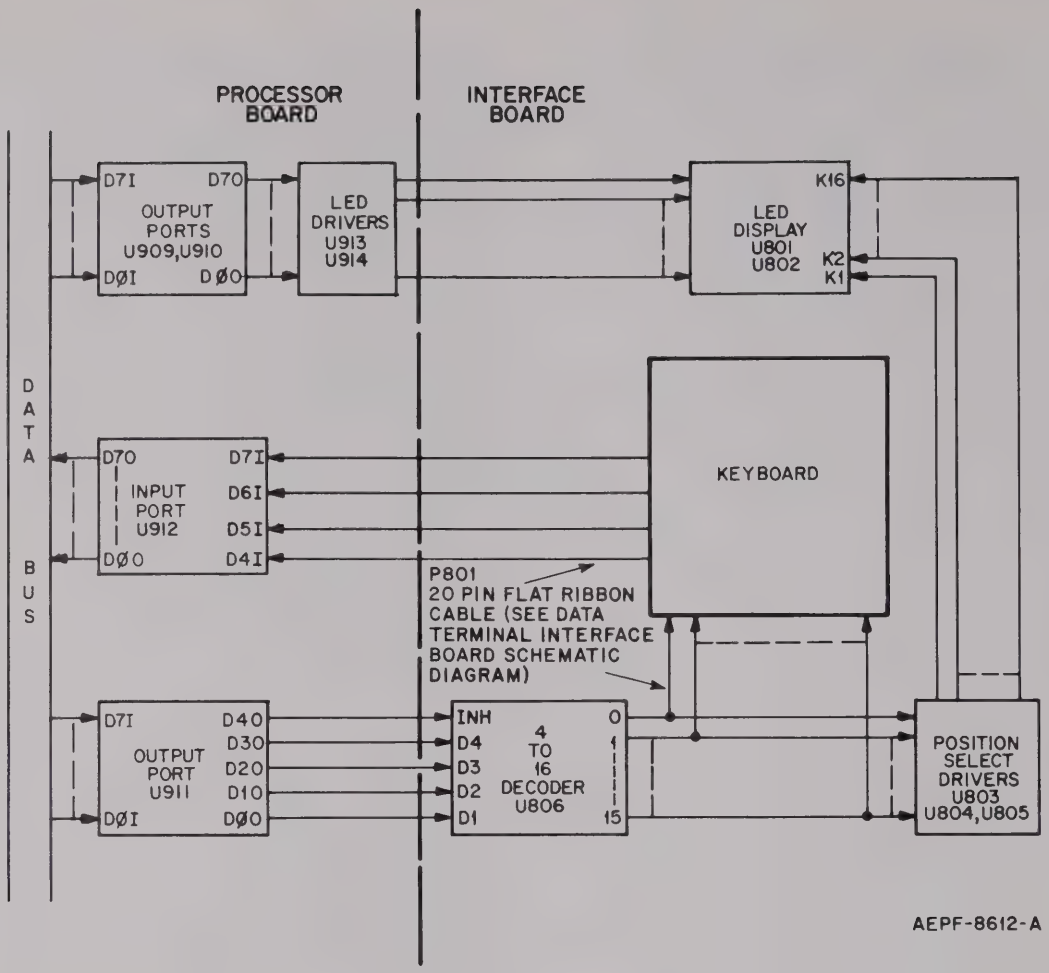


Figure 13. Block Diagram, Keyboard/Display Circuits

positioning is also controlled by the outputs from the 4-to-16 decoder (U806). Each output is applied through an associated driver-select circuit on U803, U804, or U805, which also act as current sinks for high-current ground returns for the LEDs. Under software control, the first character (position 16) is displayed, if a keyboard input has been received, and succeeding character positions from 1 to 15 are blanked by loading the output ports (U909 and U910) with all zeros. Then, when the count reaches 16 again, the output ports are again loaded with the appropriate character display information and the character is again displayed. Although the displayed character is, in effect, turned on and off, the high rate of speed at which this occurs is considerably above the flicker rate of the human eye. Other characters are displayed in the same way, with the software controlling the apparent movement of each character from right to left on the face of the display.

(4) Bit Recovery Module (U810)

Data reception over the RF link is handled by the receiver circuits of the radio portion of the data terminal. The subcarrier output from the discriminator circuit (U6) of the receiver (which contains the data information) is connected through a jumper to pin 3 of U810. The signal is first passed through a low pass filter to remove high frequency noise pulses which are invariably present in the discriminator output. Pin 23 can be used as a test point for examining the filtered signal. From the filter the signal is coupled to the tracking circuits which integrate and remove the dc level component so that the bias level shifts in accordance with any shift in the subcarrier signal. A limiter op amp (U807B) receives the output from the first stage in the tracking circuits (normal threshold level) on its + input, while the - input to U807B is received from pin 7 (data output) of U810. This second

input is developed by subsequent stages in the tracking circuits and an output shaper circuit. The limiter corrects for slow transitions around the zero crossings of the subcarrier data signal so that steep rising and falling edges are present at the output. This arrangement helps to eliminate any ambiguities between successive 1's and 0's in the data signal. Thus, if the dc level of the signal rises or falls, the bias level on the + input of the limiter also rises and falls accordingly. In effect, the tracking circuits and limiter optimize the symmetry of the signal under all operating conditions. The result is to provide a true digital input to the subcarrier demodulator circuits (module U809). Since the waveform from the output of the limiter swings between 0 and +7.5 V, a voltage divider (R802 and R803) is used to change the voltage level in the input of the demodulator to the normal logic levels of 0 to +5.5 V.

If the jumper JU801 normally connected between input (R) and pin 3 of the bit recovery module is switched from (R) to (T) (pin 20 of U810), a test input is provided for checking the operation of the following circuits without the need for an external signal source. In this case the Q signal from the processor board, which represents an internally generated data signal, is connected via pin 19 to a shaper/amplifier and level shifting circuit in U810. This signal is then connected to the low pass filter (via input (T)) to provide the self-test arrangement.

(5) Demodulator Circuits (U809)

The demodulator circuits for extracting the original baseband data from the subcarrier signal are contained on hybrid module U809, along with the clock circuits (see preceding paragraph (2)). In order to understand the operation of the demodulator, it is helpful to first consider the method of modulating (encoding) the subcarrier data signal. The technique used here, differential phase shift keying (DPSK), is a technique in which the reference signal phase for a given keying interval (data bit) is the phase of the signal during the preceding keying interval. The idealized waveforms shown in the timing diagram of Figure 14 illustrate both the encoding and decoding schemes for implementing DPSK. For encoding the original baseband data (waveform 1), the method shown (for explanation purposes only) uses a J-K flip-flop which is clocked by a 1200 Hz square-wave signal (waveform 2). The Q output of the flip-flop (waveform 3) can then be considered to be the differentiated output of the input data signal. By taking this differential signal and passing it through an exlusive-OR gate with the same clock signal, the DPSK signal results, as shown in waveform 4. If raw baseband data were used to modulate the RF carrier directly, it would result in very low frequencies when long series of 1's or 0's were encountered in the data bit stream. This would be undesirable in that shifts would occur in the receive circuits bias, resulting in zero crossing ambiguities. The above encoding technique is shown as being derived using a J-K flip-flop and exclusive-OR gate for explanation purposes only. Actual derivation in the terminal is accomplished via the MPU under software control.

For demodulating the DPSK signal, all that is necessary is to take the received or recovered data signal and run it through another exclusive-OR gate with the same signal delayed one bit time. This is shown in the idealized waveforms 5, 6, and 7 on Figure 14, so that the demodulated DPSK signal is an exact replica of the original baseband data (waveform 1). Thus, the received signal from the bit recovery module (U810) and the limiter op amp (U807B) is applied to the demodulator circuits at pin 6 of U809. The demodulator consists of three IC counters which collectively function to provide the one-bit delay needed to perform the decoding process. The first counter is a presettable 16-stage unit, the second is a presettable 13-stage unit, and the third counter is a 64-stage unit. This provides a 93-stage delay register which, when clocked at the 111.6 kHz rate, gives the required one-bit delay; i.e., the data bit rate of 1200 bits per second divided into the 111.6 kHz clock rate (dictated by the system requirements in the binary ID decoder) gives a result of 93. The output from the 93-stage delay register is passed through the exclusive-OR gate with the undelayed signal, as described previously, to provide the recovered data output at pin 11 of U809. A low-pass filter circuit is used at the demodulator output to eliminate any short time-duration pulses because of clock and time differences. Thus, successive bits in the data stream are compared for phase relationship to recover the original baseband signal according to the following rule:

- if the two successive bits are in phase, data bit output = 0
- if the two successive bits are out of phase, data bit output = 1

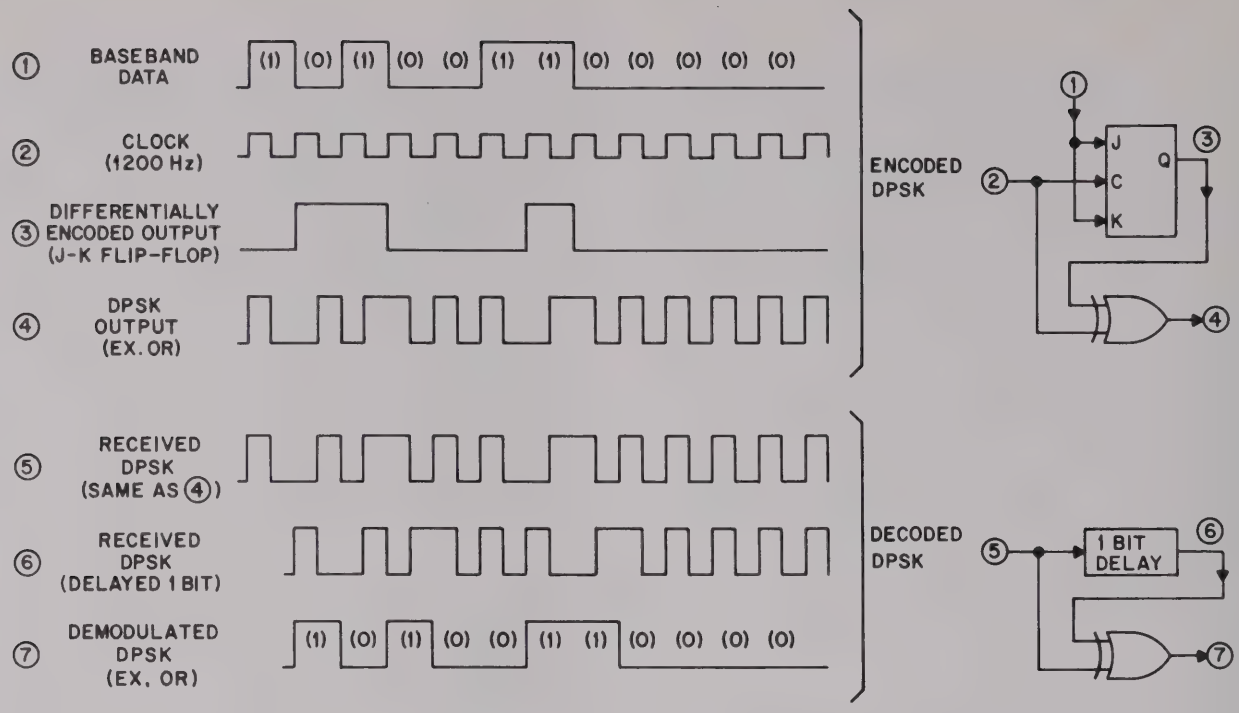

① BASEBAND DATA
(1) (0) (1) (0) (0) (1) (1) (0) (0) (0) (0) (0)
② CLOCK (1200 Hz)
③ DIFFERENTIALLY ENCODED OUTPUT (J-K FLIP-FLOP)
④ DPSK OUTPUT (EX. OR)
ENCODED DPSK
J
C
K
Q
⑤ RECEIVED DPSK (SAME AS ④)
⑥ RECEIVED DPSK (DELAYED 1 BIT)
⑦ DEMODULATED DPSK (EX. OR)
(1) (0) (1) (0) (0) (1) (1) (0) (0) (0) (0)
DECODED DPSK
1 BIT DELAY
AEPF-8614-0

Figure 14. Timing Diagram, Differential Phase Shift Keying

(6) ID/Sync Decoder Module (U812)

The recovered data output from the demodulator circuits on U809 is connected to the processor board, where it is passed through a buffer circuit and then returned to the interface board via interboard connector pins 23 and 24. The buffered signal is used as the input to the ID/sync decoder module (pin 6 of U812), which detects the ID code associated with a particular data terminal and synchronizes the operation of the terminal for subsequent data reception. (Refer to the basic functional description for formats associated with the ID codes.)

ID code detection is accomplished by a special LSI chip on U812 which acts as a digital matched filter, sensitive only to the particular code sequence dictated by the programmed code plug (U813). In general, the decoder logic correlates the programmed sequence and detects the input signal based upon a predetermined fixed percentage of correct samples. When there is correspondence between the two sequences (data input and code plug output), the detector shifts to the second word of the ID code, which is then checked in a manner similar to the first. If there is correspondence with the second word, the alerting logic provides an interrupt signal to the processor board. Thus, the decoder continuously samples the received signal when information is being transmitted and, when a valid detection occurs, a synchronized interrupt signal is generated.

Inputs to the decoder consist of the data (pin 6), clock, at 223.2 kHz (pin 5), and the 6-bit outputs from the code plug (pins 7-12). The code plug information is loaded into the decoder circuitry upon interrogation by the decoder logic. This is accomplished initially by the word select signal (pin 13), which selects either the first or second word of the ID code as required; see Figure 15.

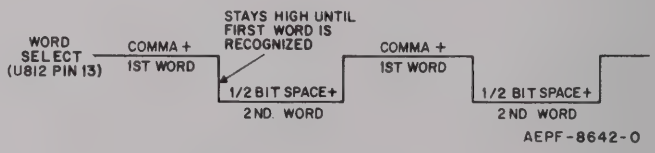

WORD SELECT (U812 PIN 13)
COMMA + 1ST WORD
STAYS HIGH UNTIL FIRST WORD IS RECOGNIZED
1/2 BIT SPACE + 2ND. WORD
COMMA + 1ST WORD
1/2 BIT SPACE + 2ND WORD
AEPF-8642-0

Figure 15. Word Select Signal

Code plug information is loaded into the decoder, six bits at a time. A code group select signal (pin 4) is used to select the appropriate six bits of the code word (Figure 16). Finally, the code plug strobe signal (pin 3) allows the information that has been selected (ID word 1 or 2, and 6-bit code group 1 or 2) to be brought out to the decoder input lines (pins 7-12).

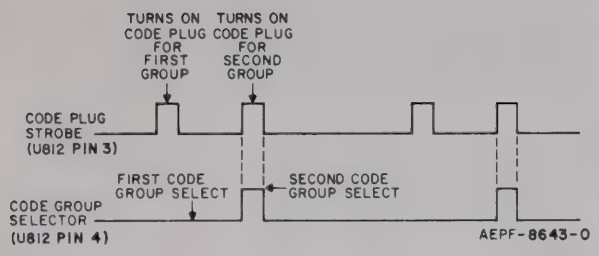

TURNS ON CODE PLUG FOR FIRST GROUP
TURNS ON CODE PLUG FOR SECOND GROUP
CODE PLUG STROBE (U812 PIN 3)
FIRST CODE GROUP SELECT
SECOND CODE GROUP SELECT
CODE GROUP SELECTOR (U812 PIN 4)
AEPF-8643-0

Figure 16. Code Plug Control Signals

A parallel load signal (internal to the decoding logic) allows the code plug information to be loaded into a storage register. As the 12 bits of ID code information are being loaded, the logic generates the 11 bits of parity required to complete the code. The total of 23 bits is then held as the reference source for comparison with the received input data stream.

The data input at pin 6 is loaded into a 92-stage recirculating asynchronous register under control of a 2400 Hz sample clock, which is obtained by dividing the decoder clock input at pin 5 by 93. Since the incoming data rate for the ID words is 600 bits per second, four samples per bit are made as the information is recirculated in the 92-stage register. Each 23-bit ID word is shifted for 92 clock pulses, recirculated, and then compared serially with each bit of the code plug register output. Since each data bit is sampled four times (23 x 4 = 92), there is a one-to-one correspondence with the code plug information.

An exlusive-OR gate compares the two signals and determines the number of differences (errors), which are counted and stored in a register. If the number of errors is less than the allowed maximum, a correlation between the two codes is indicated. If there is correlation, and the first word of the ID code is detected, the decoder begins looking for the second word of the code. The word select and code group select signals then set up the appropriate code plug outputs. The second word is detected in the same way as the first word.

An overall timing diagram of the decoder operation is given in Figure 17. Depending on the particular format of the received signal, the second word detect signal can represent any one of four different combinations of words 1 and 2. These are designated as AB, $\overline{A}B$, $A\overline{B}$, or $\overline{A}\overline{B}$, in which A represents word 1, $\overline{A}$ represents word 1 inverted, B represents word 2, and $\overline{B}$ represents word 2 inverted. Refer to the basic functional description for the meaning of the various detect signals.

Since these detect signals can occur at any one of three possible times, the "window" for encompassing these times extends from the 92nd to the 95th count of the sample clock. As shown in Figure 17, the ID detect pulse is generated at the 95th count, which then forces the $\overline{\text{DETECT INTERRUPT}}$ line (pin 22 of U812) low. This effectively provides for a synchronized ID detect signal. However, to provide some time for the circuits on the processor board to react to the interrupt signal, the ID detect signal, in conjunction with the CODE GROUP SELECT signal, starts a 7-stage counter in the decoder module. At the end of the count, the Q6 output from the counter presets the D input of a flip-flop which causes the $\overline{\text{DETECT INTERRUPT}}$ signal to again go high at the next sample time. This is interpreted by the processor (via interconnect pin 22) as the completion of the delayed sync period and indicates that valid message data is to follow.

Detect lines AB and $\overline{A}B$, which represent a poll for data and outbound message alerts respectively, are interconnected between modules U812 and U809 so as to utilize an existing OR gate on U809. The input at pin 21 of U812 then represents either one of these detects and is used to reset the $\overline{\text{DETECT INTERRUPT}}$ line low. Signal AB is detected by sampling the flag line input ($\overline{EF2}$) to the MPU without a corresponding signal from the other three detect signals. These latter signals are latched to provide a signal of sufficient duration for application to the input port (U912) on the processor board. Signal $\overline{A}B$ is connected between pins 18 and 27 of U812 and, after being latched by a flip-flop in the module, appears at pin 28 and board interconnect pin 17. Both signals $A\overline{B}$ and $\overline{A}\overline{B}$ are connected to the processor board, via pins 5 and 3 respectively, where they are latched by flip-flops U904A and U904B.

f. Data Terminal Processor Board
(Refer to Figures 41 and 45)

(1) Power Turn-On Sequence

When the radio on/off switch is turned on, 4.6 V from a regulator circuit in the radio (U7) is applied to the data terminal via the inter-

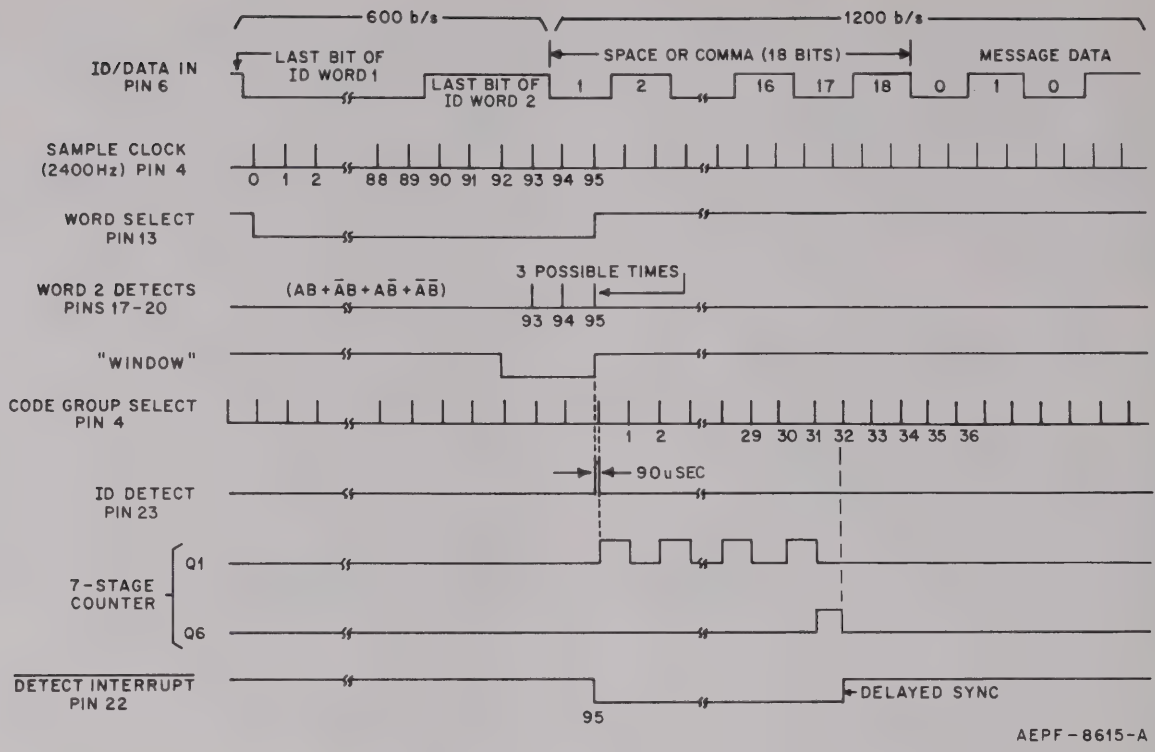


Figure 17. Timing Diagram, ID/Sync Decoder

face board, turning the 5.5 V regulator on. The 7.5 V from the battery (fuse) is applied directly to the terminal's display drivers and to the regulator circuit on module U811, of the interface board. The resulting 5.5 V regulated output from the regulator is then applied as a single voltage source for the entire processor board. The 5.5 V level is defined as the logic high (binary 1) level, while ground is defined as the logic low (binary 0) level.

A power reset signal is derived by an RC time constant circuit across the 5.5 V line on module U812 of the interface board. The duration of this signal is set to a value greater than 100 ms to provide adequate set-up time for the decoder circuits on the interface board.

Inverter U903A inverts the power reset signal to produce signal $\overline{\text{CLEAR}}$, which is applied to the MPU and the I/O ports. This initializes the circuits to provide the proper starting point for a new operation. When $\overline{\text{CLEAR}}$ goes high sometime after 100 ms, the MPU forces all zeros on the 8-bit address bus and memory location 0 is selected in the EPROM. Mapping of the EPROM is such that the starting or initialization routine begins at location 0.

(2) Microprocessor and Memory Units

Internal operation of the microprocessor (U906) and memory (RAM and EPROMs, U917 through U921) units is performed by complex integrated circuits which are not covered here. The following paragraphs, therefore, are concerned only with descriptions of the input and output signal connections from these devices.

D0 to D7: 8-bit bi-directional data bus lines. These lines are used for transferring data between the memory, MPU, and I/O ports.

N0 to N2: (I/O Command) Issued by an I/O instruction in the MPU to signal the I/O control logic of a data transfer between memory and an I/O port or an optional I/O device (light pen). These lines provide for device selection and are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in a register in the MPU.

A0 to A7: 8-bit memory address bus lines. The higher-order byte of a memory address appears on the address lines first. Those bits required by the memory system are strobed into external address latches by a timing pulse (TPA). The lower-order byte of the address then appears on the address lines after the termination of TPA. Latching of the six higher-order address bits permits a memory system of up to 16,384 bytes, although fewer than this are used in the terminal.

TPA, TPB: (Timing Pulses) Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by the memory system to latch the higher-order byte of the memory address and to time interaction with the data bus.

CLK: Input for the externally generated single phase clock. The clock frequency is 2.6784 MHz and is counted down internally to eight clock pulses per machine cycle.

$\overline{MRD}$: (Read Level) A low level on $\overline{MRD}$ indicates a memory read cycle. It is used to control 3-state outputs from the addressed memory which have a common data input and output bus. It is also used to indicate the direction of data transfer during an I/O instruction.

$\overline{MWR}$: (Write Pulse) A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

Q: A single bit output which can be set or reset under program control. It is used to represent the serial data bit stream during transmitting operations, and is set or reset between the trailing edge of TPA and the leading edge of TPB.

$\overline{INT}$: Activated by a 2400 Hz clock signal from the interface board. It is used in conjunction with data input operations to synchronize the writing of new data into the MPU and RAM.

$\overline{EF1}$ to $\overline{EF4}$: (Flag Bits) These levels enable the I/O devices to transfer status information to the MPU. They are tested by the program during the execute phase of an instruction.

$\overline{WAIT}$, $\overline{CLEAR}$ (Control Lines) Provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
Low	Low	Load
Low	High	Reset
High	Low	Pause
High	High	Run

The functions of the modes are defined as follows:

Load

Holds the MPU in the "idle" execution state and allows an I/O device to load the memory without the need of a "bootstrap" loader.

Reset

Internal registers are reset and zeros are placed on the data bus. Timing pulses TPA and TPB are suppressed while reset is held and the MPU is placed in the execution state. The first machine cycle after termination of reset is an initialization cycle. Interrupt servicing is suppressed during the initialization cycle.

Pause

Stops the internal MPU timing pulse generator on the first negative transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

WAIT, CLEAR (Control Lines) (cont'd)

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the MPU resumes operation on the first negative transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle.

(3) Memory Circuits

Decoding elements U915A and U915B are 1-out-of-4 decoders that provide for addressing the memory units. For the EPROMs, U915A receives address bits A11 and A12 from the address bus and produces three outputs ($\overline{Q0}$, $\overline{Q1}$, and $\overline{Q2}$), which select EPROMs U919, U920, and U921 respectively. Selection is accomplished when the $\overline{Q}$ signals from the decoder are low, via transistor drivers (Q901, Q902, and Q903). The transistors, when driven on by the $\overline{Q}$ signal, provide for power strobing of the EPROM chips; i.e., with the chip select line ($\overline{CS}$) of each EPROM grounded, chip selection is implemented by the application of V_{CC} to pin 24, via the respective transistor driver, of the selected memory chip. As an option feature on later version processor boards, an additional power switching circuit consisting of transistor Q904 and resistor R922 driven by $\overline{Q3}$ of U915A is provided. This circuit along with option jumper JU902 can be used to enable use of a 4K x 8 EPROM in position U921 instead of a 2K x 8, thereby expanding program capacity to 8K.

Decoder U915B provides selection of the RAM by applying the $\overline{Q3}$ output directly to the chip select inputs ($\overline{CS}$) of U917 and U918. Address bit A13 is used to select either the RAM or EPROM. If this bit is high, it enables the decoding circuits for the RAM, so that memory addresses greater than hexadecimal 2000 (those reserved for the RAM) are selected. At the same time, bit A13 is applied to pin 1 of U915A to act as an inhibit on the EPROM decoding circuits. Circuit components CR901, R903, C902, and U901E form a pulse stretching circuit to lengthen the $\overline{MRD}$ signal from the microprocessor. This is necessary because of the nature of the RAM chips, which require an additional 600 ns of chip select time. Diode CR901 passes the positive-going edge of $\overline{MRD}$ and, when $\overline{MRD}$ goes negative, the RC time constant of R903 and C902 causes a slow decay at the input of driver U901E. This effectively provides the needed stretching of $\overline{MRD}$ for the extra 600 ns.

Circuit element U916 contains six flip-flops which serve as external address latches for the higher-order address byte. Address bits A0 through A5 are latched during timing pulse TPA, after which output A8 through A13 are available for use as inputs to the memory.

(4) Input/Output Ports

These units provide the input/output paths between the processor and interface boards. Each of the ports use the same CMOS IC package, but U909, U910, and U911 function as output ports, while U912 functions as the single input port. Mode control is provided simply by connecting pin 2 of the port to either ground or +5.5 V. If this line is high (tied to +5.5 V), the unit serves as an output device; if the line is low (grounded), the unit is configured as an input port.

Selection of an I/O port is controlled by the MPU output N lines (N0 through N2). These three bits are set by an instruction and are connected to a binary-to-BCD decoder (U902), so that individual select lines (N1 through N7) are available for identifying I/O devices. Thus, the three output ports U909, U910, and U911 are selected by lines N1, N2, and N3 respectively. (The other N lines (N4, N5, N6, and N7) are used for selecting and controlling optional peripheral devices such as the light pen.)

The N lines can be shared between input and output ports since they are configured for one-way operation by the mode control line (pin 2). Therefore, N1 is also used to select input port U912. The chip select inputs (CS1 and CS2) associated with each port then determine which port is used. For an output operation, the $\overline{MRD}$ signal is low (output memory read operation) which satisfies the condition required for selecting an output port; i.e., chip select signal $\overline{CS1}$ at pin 1 of U909 is low. Since the chip select input at pin 1 of the input port (U912) requires a high input for operation (signal CS1), this port will be blocked when $\overline{MRD}$ is low. Conversely, for a memory write (input) operation, signal $\overline{MRD}$ will be high and U912 will be selected.

Each of the I/O ports contain an 8-bit data register which is connected to a set of eight 3-state output drivers. These output drivers permit the ports to appear as high-impedance devices to the data bus when they are not in use. For an output operation, inputs D0 I through D7 I are connected to the data bus and the information is strobed into the 8-bit data register by the CLK input (pin 11). This input is derived directly from timing pulse TPB

which is high during the latter part of an MPU cycle. The output data then appears on output lines D0 O through D7 O and are available for use by the interface board. Output ports U909 and U910 are connected to segment drivers U914 and U913, which provide the required current for operating the 15-segment display elements of the character display on the interface board. Output port U911 provides five outputs (D0 O through D4 O) which are connected to the 4-to-16 decoder/latch circuit on the interface board for use in controlling the display. Three other outputs from U911 (D5 O through D7 O) provide software controlled signals as follows:

D5 O = Strobe Control: This signal is used to force the MPU into a quiescent state to save current drain on the battery when there is no activity in process. When an inactive condition is detected, the software forces the strobe control line high, which then gates the sample clock pulse through U905C to produce a low $\overline{\text{WAIT}}$ signal. This forces the MPU into its waiting or idle state and the low current condition is realized.

D6 O = Alert Signal: When the data terminal detects an RF input signal from the transmitter base station, it generates the $\overline{\text{DETECT}}$ $\overline{\text{INTERRUPT}}$ signal on the interface board which, in turn, sets a flag bit ($\overline{\text{EF2}}$) in the MPU. Under software control, the ALERT signal may appear on output line D6 of I/O port U911. The alert signal is fed back to the interface board where it is shaped in module U811 and then applied to the audio circuits in the receiver section of the radio.

D7 O = PTT: This signal is generated whenever an output operation involving the transmission of data from the terminal is called for. It effectively activates the transmitting circuits of the radio.

For input operations, I/O port U912 has its CLK input (pin 11) tied to +5.5 V. This makes the port appear transparent to the MPU, so that any input information appearing on the input lines (D0 I through D7 I) is available on the corresponding output data bus lines (D0 O through D7 O) when the I/O port is selected. Inputs D4 I through D7 I are connected directly to the keyboard matrix so that whenever a key is depressed, one of these lines goes high to initiate MPU control of the display operation.

Inputs D0 I through D2 I are associated with the message format detection signals from the interface board. These signals are latched by flip-flops (U904A and U904B) and applied through the input port to the data bus. One of four different message formats is then determined for the subsequent terminal operation. The input present on line D3 I is the actual recovered data from the interface board that represents the input information to the terminal for the current operation.

(5) Overall Timing Diagram

Figure 18 is an overall timing diagram of the basic MPU instruction cycle and I/O operations. Part A shows the timing for a memory read operation, in which the memory element can be either the RAM or EPROM and the destination of the data can be either the MPU or an output port. A memory write operation (into the RAM only) is shown in part B. Here, the source of the data to be written can be from the MPU or the input port. The basic clock rate of 2.678 MHz is shown for three complete MPU or machine cycles; i.e., eight clock pulses from time 0 to the next time 0 constitutes a basic machine cycle. For a memory read operation, the $\overline{\text{MWR}}$ signal remains high while the $\overline{\text{MRD}}$ signal goes low following the first timing pulse (TPA). During this time, the higher-order address bits (A1) are latched into the memory decoders, followed by the lower-order address bits (A0). When timing pulse TPB occurs, the data at the addressed storage location (RAM or EPROM) is considered to be valid and can be presented to the data bus and the MPU registers.

The shaded portions of the data waveforms indicate the period of time during which the address information on the address bus is unsettled and results in some minimum delay before the data is considered to be valid. Also notice the data waveforms are depicted as three-state signals; i.e., during the unsettled and valid data periods, the data may be high or low (indicating 1's and 0's), while during the time that no data is present on the bus the signal waveform is shown in its high impedance or open circuit state.

As indicated in Figure 18, the first cycle depicts a representative instruction fetch cycle, in which the operation code (OP code) byte of the current instruction is brought from memory to the MPU. The second cycle shows the execute phase of the instruction in which the memory is again referenced (A1 and A0) for the operand data under control of TPA and TPB. Depending on the type of instruction, the following

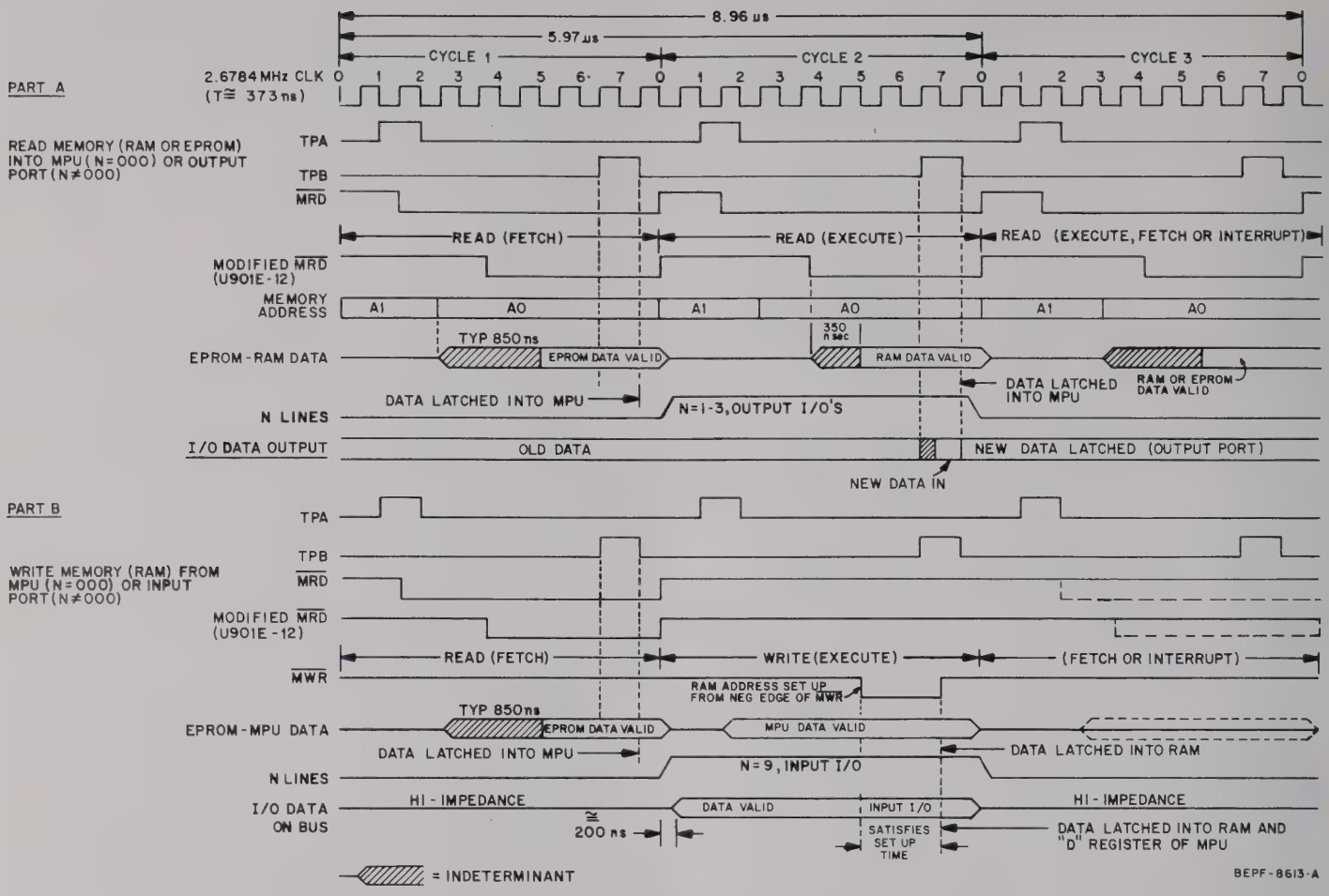


Figure 18. Overall Timing Diagram, Processor Board

third cycle can represent either the fetch phase of a new instruction, or another execute phase of an extended operation (one fetch phase plus two execute phases).

If I/O operations are involved in the execution of the instruction, the I/O port is addressed by the N lines during the second machine cycle (N bits high). Immediately after timing pulse TPB, at the beginning of the third machine cycle, the new output data is latched from the data bus into the output port. For an input operation (part B), the input port is connected in the transparent mode (no clock or latching of the data) so that whenever data is read into the port from the interface board, it is available on the data bus when the I/O port is enabled.

g. Light Pen and Interface Circuit
(Refer to Figure 19)

(1) Light Pen

Figure 19 shows a block diagram of the light pen used with the terminal. The pen contains a light source, an optical system (for directing and focusing the light beam), a transducer (that senses the light reflected from the media), and an amplifier (that converts the transducer response to a voltage output).

The pen produces an analog output that is directly proportional to the amount of light reflected by the bar code being scanned. Note that the contrast and print quality of a given media determine the peak-to-peak signal swing of the light pen analog output.

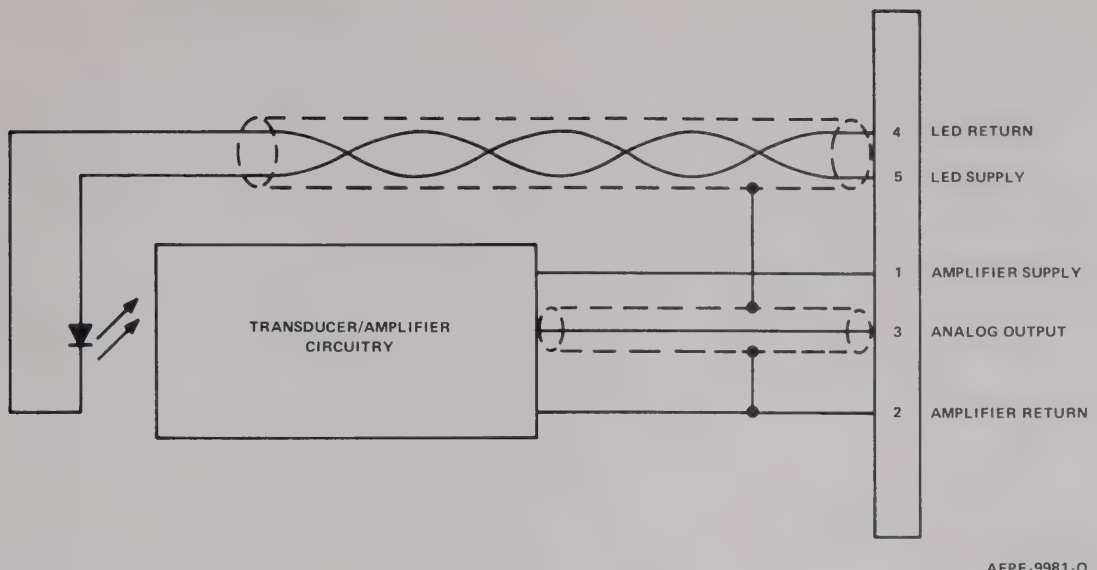


Figure 19. Light Pen Block Diagram

The pen produces a "free air" output when it is not on a reflective surface. This output, depending on the manufacturer, is approximately 0.0 V to 0.5 V. Placing the pen on a white surface produces a "white level" that is normally 100 mV above the free air level. Scanning the media produces a fluctuating output with the black levels close to the free air level (how close depends on media quality) and the white levels approximately 100 mV higher.

(2) Interface Circuit

Figure 20 shows a block diagram of the light pen interface circuitry. This circuit digitizes the analog output of the light pen by creating an adaptive threshold, which tracks the waveform when its dc component or peak-to-peak amplitude shifts. This technique is used because of the combined effect of the following factors:

- Identical light pens produce varied output characteristics, which in turn vary with temperature and LED current.
- Because the circuit is dc coupled, variations in the free air output level affect the dc operating point.
- Gain tolerance in the first stage and temperature effects on the interface circuit also affect the dc operating point.
- Adjustable or select-at-test components are not used, eliminating the need to match light pens to interface circuits.

To minimize power drain, the MPU periodically interrogates the light pen for a change from the free air level. Current switch U816-1 and Q802, under MPU control, turns the LED current (approximately 50 mA) on and off, pulsing the LED at an approximate 2.5% duty cycle. If a change from the free air level is not detected when the LED is on, it is switched off until the MPU is ready to sample again. If a change is detected, comparator U807D drives MPU input EF1 high, which then allows the LED to remain on until the data is captured.

The analog signal from the light pen is sent to the amplifier with offset stage, U807C. This device provides a gain of approximately 2.5. Diodes CR808 and CR809 in the feedback loop offset the signal toward the center of the supply range. The signal is then applied to the unity-gain sample-and-hold stage U815A, C816, and U808D. This stage protects the remainder of the circuitry from noise when the light pen is not being sampled.

The next stage is a complementary peak detector followed by high impedance buffers. The positive peak detector/buffer consists of U808A, CR803, C817, U815B, and U814A. The negative peak detector/buffer consists of U808B, CR804, C818, U815C, and U814B. Quick reset of the peak detectors, under MPU control, is provided by devices U815B and U815C. This ensures that each succeeding peak voltage value is stored without regard to the value of the preceding peak.

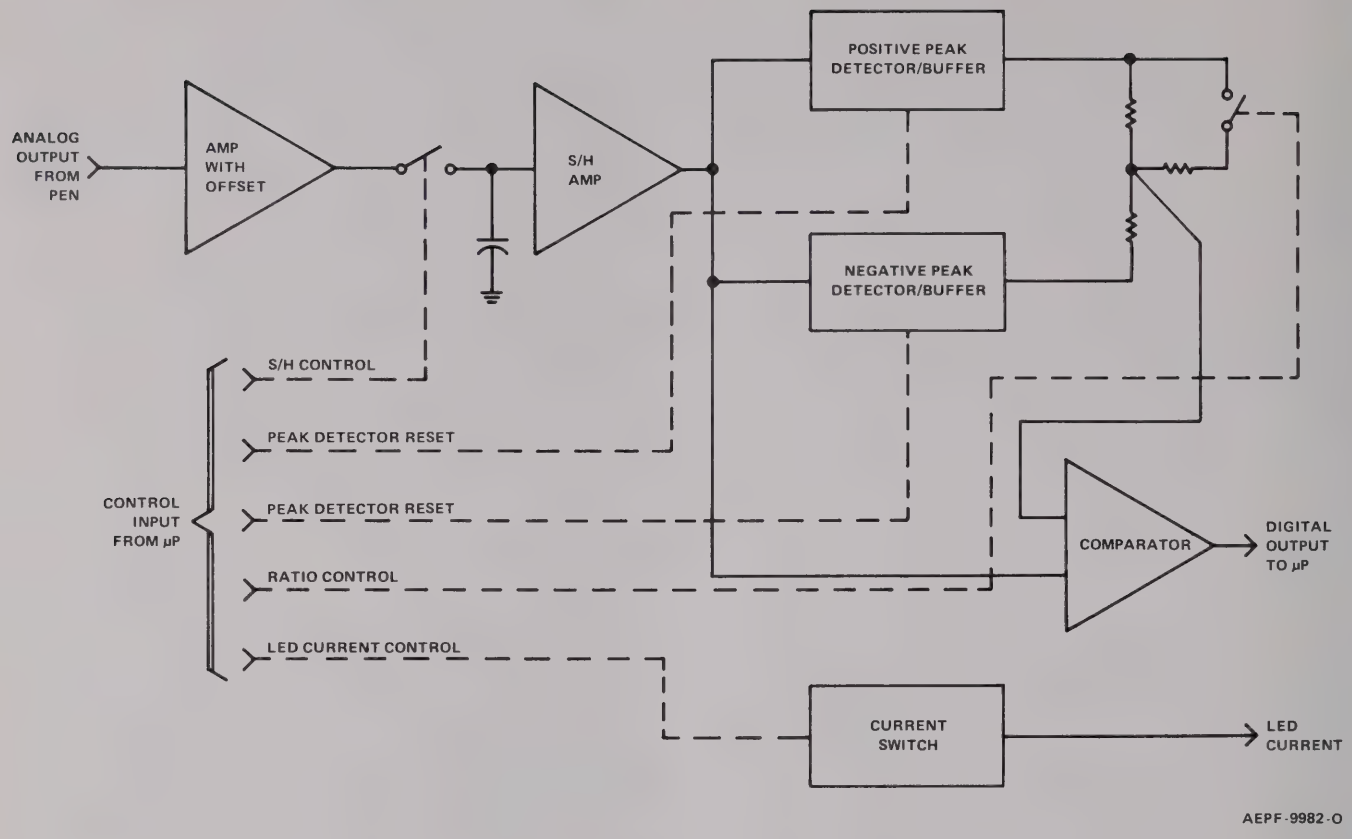


Figure 20. Light Pen Interface Circuitry

The output of this stage is applied to a voltage divider network comprised of R813, R814, R815, and U815D, that is used to set the adaptive reference for the output comparator (U807D). This reference is set somewhere between the preceding positive and negative signal peaks under control of the MPU via the use of U815D. The reference threshold can be switched at either one-third or two-thirds of the way between the two preceding peaks, via the ratio control input signal (the Q2 output of U816). When the light pen input is high (white state), the threshold is at two-thirds and when low (black state), the threshold is at one-third. This action enhances the unit's ability to read poor-contrast media. Between scans, the threshold is set at the one-third level.

To control the hysteresis of the output comparator, device U808C and diodes CR805 and CR806 are used. Without hysteresis control, the exact dc operating point of the circuit would depend on the output level of the light pen, the tolerance of the gain stage, the temperature, etc. Buffer U808C provides unity gain for the adaptive threshold. By connecting the output of U808C to the output of U807D through two back-to-back diodes and a resistor, a signal is generated. This signal is one diode drop above the threshold voltage when U807D is high, and one diode drop below the threshold when U807D is low (point K, detail A of the interface board schematic diagram, Figure 43). Fed forward, it is divided down by resistors R820 and R821 which provides U807D with a nominal 40 mV of hysteresis.

(3) Typical Data Capture Sequence

A typical data capture sequence is outlined in the simplified flow chart in Figure 21, and can be described as follows:

(a) LED current is switched on at the end of a predetermined timing interval.

(b) The sample-and-hold switch is closed, after a short settling delay, allowing the light pen output to pass through.

(c) The output of the comparator, U807D, will go high and be sensed by the MPU, if the light pen is on white or other reflective surfaces. When this action occurs, the LED is left on and the MPU prepares to collect the data. Alternatively, the output of the comparator, U807D, will not change if the light pen is not on white or other reflective surfaces. The MPU then turns off LED power and reinitiates the timing cycle.

(d) If white is sensed, the MPU waits for data to start coming in. If transitions do not occur within a certain length of time, the LED is switched off and the timing cycle is reinitiated.

(e) The negative peak detector, U808B, resets as the leading edge of each bar is detected. This occurs so that each new peak level can be detected. Additionally, the adaptive threshold ratio is switched to the one-third level. When spaces are detected, the positive peak detector resets and the adaptive threshold ratio switches to the two-thirds level.

(f) After a predetermined time interval with no detected transitions, the MPU assumes that all data has been collected. The sample-and-hold switch is then opened, the LED is switched off, and the MPU data decoding cycle begins.

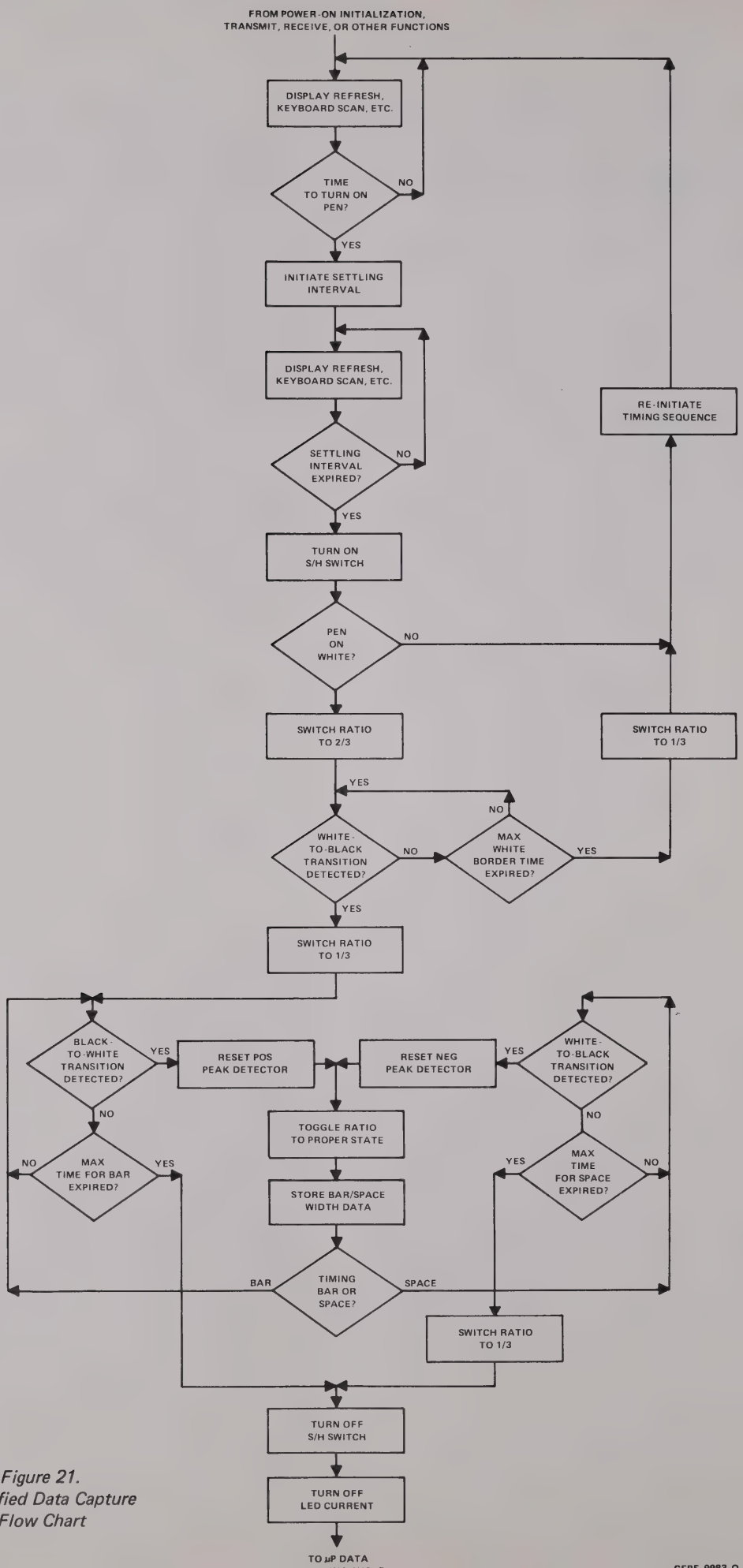


Figure 21.
Simplified Data Capture Flow Chart

DISASSEMBLY PROCEDURES

1. GENERAL

An exploded view of the RF data terminal is shown in Figure 22. It illustrates how the various major units of the terminal can be separated and disassembled to facilitate servicing of the terminal. Before attempting any of the following disassembly procedures, remove the unit from its carrying case, make sure it is turned off, and remove the battery, as described in the operating instructions.

2. REMOVING AND SEPARATING THE FRONT COVER ASSEMBLY

a. Loosen the four captive screws (15) on the back of the keyboard and processor housing assembly until the front cover assembly (1) is free.

b. Detach the 20-conductor ribbon connector (5) from the back of the keyboard assembly.

c. Detach the 4-conductor connector (2) from the speaker.

d. Remove the keyboard assembly.

e. To separate the keyboard and touch pad assembly (20), remove the four pan-head screws (3) from the back of the front cover assembly.

3. REMOVING AND SEPARATING THE PROCESSOR AND INTERFACE BOARDS

a. Unplug the 16-pin connector (6) from the top (interface) board (11).

b. Lift the circuit board assembly from the housing back plate (13).

c. Separate the interface board (11) from the processor board (12) by removing the clips (4) on each side of the boards.

4. REMOVING AND SEPARATING RADIO SECTION FROM TERMINAL

a. Loosen the five captive screws (17) on the back cover (16) until the cover is free. There is a captive washer on each screw which should not be removed, since the washer protects the cover against excessive pressure from the processor housing studs.

b. Separate the processor housing back plate (13) from the radio by lifting the plate and its mounting studs (14) away from the radio frame.

c. Guide the interface board connector (6) through the rectangular hole in the processor housing back plate. If the unit is equipped with the light pen option, also guide the light pen connector (18) through the rectangular hole.

d. Guide the socket half of the speaker connector (2) through the small hole in the processor housing back plate.

5. SERVICING THE RADIO MODULES

With the radio section separated from the rest of the terminal as described above, access to the radio modules can be achieved by simply removing the pressure pad (19).

6. REMOVING THE RADIO CIRCUIT BOARD FROM THE RADIO FRAME

a. Remove the keyboard and processor housing assembly and back cover as previously explained.

b. Unsolder the B+ and B- leads at the top of the radio circuit board. These leads are soldered to pins on the back side of the board, behind module U105.

c. Unsolder the wires connecting the antenna jack to the radio circuit board in two places.

d. Unsolder ground wire at bottom of circuit board.

e. For convenience, remove module U104.

f. Place the radio on the bench (modules up) and with the operating controls away from you.

g. Pick up the radio with one hand on each side of the housing (near the center of each side) and with the thumbs pressing against the preselector on the circuit board.

CAUTION

When the board and module assembly is released from the housing, it is still attached to the control flex circuit and may damage the flex circuit if the weight is not supported. Hold the radio close to the bench or other surface as instructed in the following step. Remove the heavy modules from the board to reduce the weight.

h. Hold the radio in a horizontal position about one inch above the bench or table and gently pull the sides of the housing apart while gently pressing on the preselector with the thumbs. When the sides have been flexed far enough, the board will clear the retaining notches on the sides of the housing.

i. Carefully unfold the circuit board while supporting its weight with one hand. The board will still be attached to the control flexible circuit and the multi-freq flexible circuit (if applicable).

7. REMOVING THE CONTROL FLEX CIRCUIT

Do not remove the control flex circuit from the housing unless a defective part or control requires replacement. If necessary, refer to the repair and replacement procedures in a later section of this manual.

8. REMOVING THE POWER FLEX CIRCUIT

Refer to the exploded view (Figure 22) and proceed as follows.

a. Remove the battery, keyboard and processor housing assembly, and back cover from the unit.

b. Unscrew the fuse cap and remove the fuse.

c. Remove the two battery contacts, held by screws in the bottom of the radio section.

d. Remove modules at the top of the radio section to provide access to the volume control.

e. Remove modules at the bottom to provide clearance for removing the flex circuit.

NOTE

In terminals with optional boards at the bottom, it may be necessary to carefully remove the radio circuit board before removing the flex circuit.

f. Carefully unsolder the flex circuit from the volume control contacts.

g. Unsolder the red (B+) and the black (B-) wires from the radio circuit board.

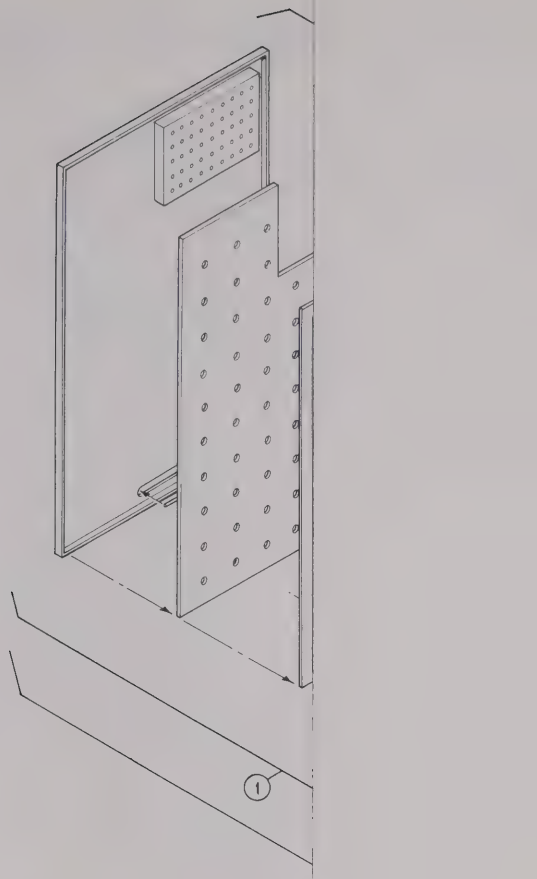
h. Using the module pusher tool, carefully push each fuse clip out by pushing on them from the bottom of the radio section.

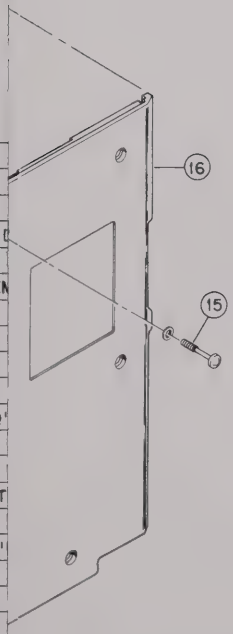
i. The flex circuit is now held only by tape to the side of the housing and can be peeled loose.

NOTE

If the fuse clips must be replaced, refer to the repair and replacement procedures in a later section of this manual.

j. Reverse the above procedure to replace the power flex circuit. If a new flex circuit is being installed, bend it in three places using the old flex circuit as a guide.





ITEM	DESCRIPTION
1	FRONT COVER ASSEMBLY
2	SPEAKER CONNECTOR
3	PAN-HEAD SCREW (#2)(4 REQ'D
4	CLIP, P.C. BOARD (2 REQ'D)
5	RIGHT ANGLE CONNECTOR ASSEM
6	RADIO INTERFACE CONNECTOR
7	MICROPHONE
8	LIGHT PEN
9	SPEAKER
10	PAN-HEAD SCREW (#4)(2 REQ'
11	INTERFACE BOARD
12	PROCESSOR BOARD
13	PROCESSOR HOUSING BACK PLAT
14	STUD (5 REQ'D)
15	CAPTIVE SCREW (4-40)(9 REQ'
16	BACK COVER
17	GASKET
18	LIGHT PEN CONNECTOR BOARD
19	PRESSURE PAD
20	KEYBOARD AND TOUCH PAD ASSEM
21	LENS (LED DISPLAY)
22	FRONT COVER
23	CONNECTOR, ELASTOMER (2 RE
24	CLIP,-SPEAKER
25	SPEAKER ASSEMBLY
26	INTERFACE CABLE ASSEMBLY

EEPF-8743-A

Figure 22. Disassembly Drawing

CAUTION

When the board and module assembly is released from the housing, it is still attached to the control flex circuit and may damage the flex circuit if the weight is not supported. Hold the radio close to the bench or other surface as instructed in the following step. Remove the heavy modules from the board to reduce the weight.

h. Hold the radio in a horizontal position about one inch above the bench or table and gently pull the sides of the housing apart while gently pressing on the preselector with the thumbs. When the sides have been flexed far enough, the board will clear the retaining notches on the sides of the housing.

i. Carefully unfold the circuit board while supporting its weight with one hand. The board will still be attached to the control flexible circuit and the multi-freq flexible circuit (if applicable).

7. REMOVING THE CONTROL FLEX CIRCUIT

Do not remove the control flex circuit from the housing unless a defective part or control requires replacement. If necessary, refer to the repair and replacement procedures in a later section of this manual.

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Refer to the exploded view (Figure 22) and proceed as follows.

a. Remove the battery, keyboard and processor housing assembly, and back cover from the unit.

b. Unscrew the fuse cap and remove the fuse.

c. Remove the two battery contacts, held by screws in the bottom of the radio section.

d. Remove modules at the top of the radio section to provide access to the volume control.

e. Remove modules at the bottom to provide clearance for removing the flex circuit.

NOTE

In terminals with optional boards at the bottom, it may be necessary to carefully remove the radio circuit board before removing the flex circuit.

f. Carefully unsolder the flex circuit from the volume control contacts.

g. Unsolder the red (B+) and the black (B-) wires from the radio circuit board.

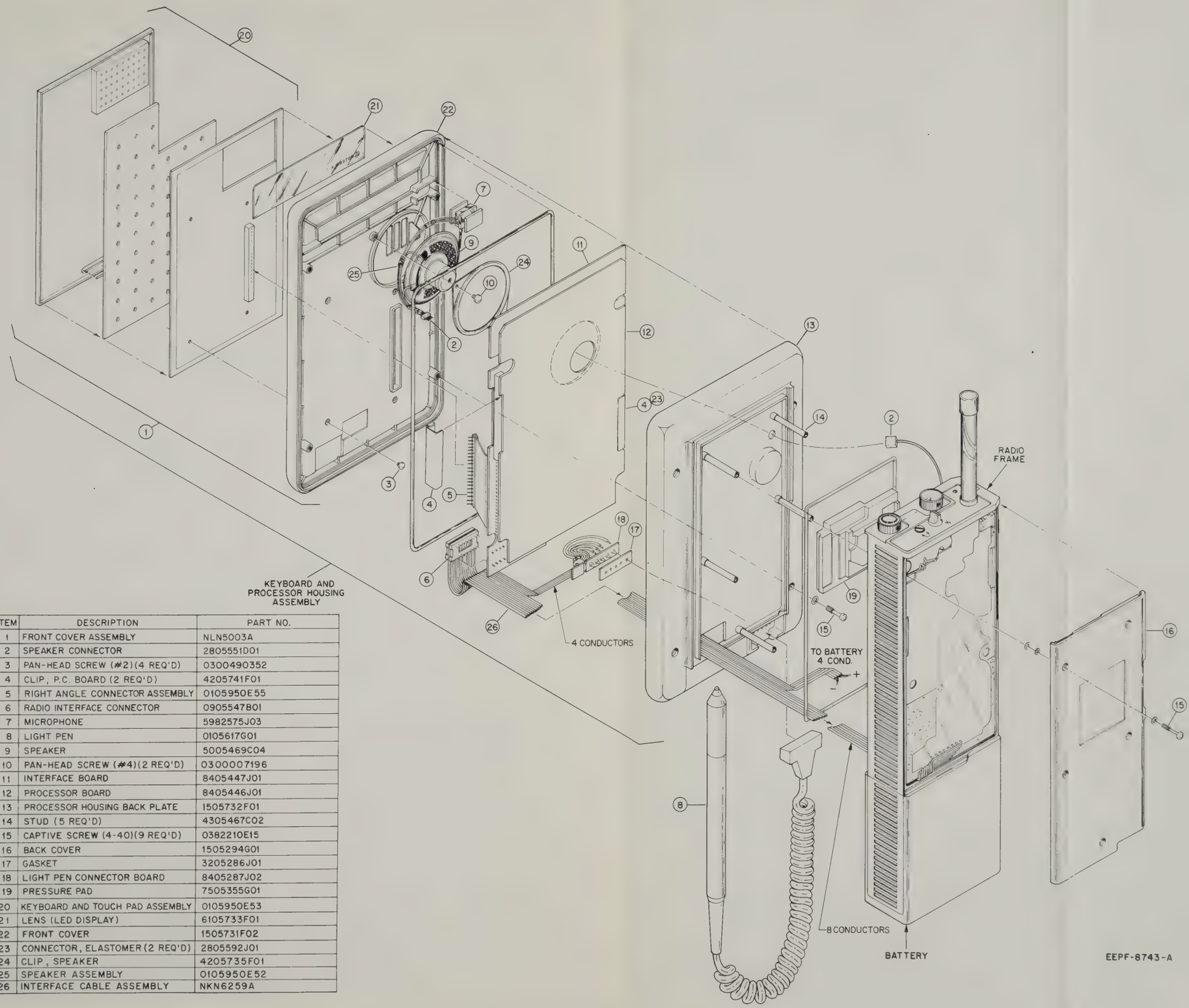
h. Using the module pusher tool, carefully push each fuse clip out by pushing on them from the bottom of the radio section.

i. The flex circuit is now held only by tape to the side of the housing and can be peeled loose.

NOTE

If the fuse clips must be replaced, refer to the repair and replacement procedures in a later section of this manual.

j. Reverse the above procedure to replace the power flex circuit. If a new flex circuit is being installed, bend it in three places using the old flex circuit as a guide.



ITEM	DESCRIPTION	PART NO.
1	FRONT COVER ASSEMBLY	NLN5003A
2	SPEAKER CONNECTOR	2805551D01
3	PAN-HEAD SCREW (#2)(4 REQ'D)	0300490352
4	CLIP, P.C. BOARD (2 REQ'D)	4205741F01
5	RIGHT ANGLE CONNECTOR ASSEMBLY	0105950E55
6	RADIO INTERFACE CONNECTOR	0905547B01
7	MICROPHONE	5982575J03
8	LIGHT PEN	0105617G01
9	SPEAKER	5005469C04
10	PAN-HEAD SCREW (#4)(2 REQ'D)	0300007196
11	INTERFACE BOARD	8405447J01
12	PROCESSOR BOARD	8405446J01
13	PROCESSOR HOUSING BACK PLATE	1505732F01
14	STUD (5 REQ'D)	4305467C02
15	CAPTIVE SCREW (4-40)(9 REQ'D)	0382210E15
16	BACK COVER	1505294G01
17	GASKET	3205286J01
18	LIGHT PEN CONNECTOR BOARD	8405287J02
19	PRESSURE PAD	7505355G01
20	KEYBOARD AND TOUCH PAD ASSEMBLY	0105950E53
21	LENS (LED DISPLAY)	6105733F01
22	FRONT COVER	1505731F02
23	CONNECTOR, ELASTOMER (2 REQ'D)	2805592J01
24	CLIP, SPEAKER	4205735F01
25	SPEAKER ASSEMBLY	0105950E52
26	INTERFACE CABLE ASSEMBLY	NKN6259A

Figure 22. Disassembly Drawing

TEST EQUIPMENT AND SERVICE AIDS

1. GENERAL

This section describes the test equipment and service aids required for maintaining the portable data terminal. See your Motorola sales representative for aid in ordering test equipment. He will analyze your requirements and help you select the latest available equipment to suit your individual needs. He can also advise you of the new test equipment and service aids that become available after the printing of this manual.

2. TEST EQUIPMENT

Refer to the list of test equipment in Table 5. Battery operated test equipment is recommended when available. The listed items or equivalents may be used.

3. SPECIAL SERVICE AIDS

Several service aids have been designed especially for servicing the terminal; see Table 6. These aids are available from the Motorola Communications Division Parts Department, or from Motorola National Data Services. Refer to the Replacement Parts Ordering page at the back of this manual.

4. ST1175 DUMMY BATTERY BLOCK

The ST1175 Dummy Battery Block attaches to the unit like a battery, but contains a cable for connecting to an external 7.5-volt power supply. An overvoltage protection circuit is built into the ST1175 for protecting the unit if greater than 9.0 volts is applied from the external power supply. The battery block is also internally fused at about 4 amperes to protect the unit. A current-limiting power supply is recommended, set at 4 amperes maximum.

Table 5. Test Equipment

MOTOROLA MODEL NO.	NAME	CHARACTERISTICS	APPLICATION
R1200	Service Monitor	--	Signal generator and frequency/deviation meter for wide-range troubleshooting and alignment in radio section.
S1347 or S1348	DC Power Supply	0-20 Vdc, 0-5 Amps, Current limited.	Bench supply for 7.5 Vdc.
S1053	AC Voltmeter	1 mV-300 V, 10 megohm input impedance.	Audio voltage measurements
S1063 or R1001	DC Multimeter Digital Multimeter	200 mV min full scale, 1 uA-300 mA, 10 megohms input resistance, 0.2 ohm - 50 megohm resistance.	DC voltage, current, and resistance measurements.
SLN6055 with SLN6083 termination. --- or S1339	RF Probe --- RF Millivoltmeter	0.3 to 10 volts full scale, 10 MHz to 400 MHz --- 100 uV to 3 V RF 10 kHz to 1.2 GHz	Plugs into S1063 DC Multimeter for making RF measurements.
R1004	Dual-Trace Oscilloscope	10 MHz bandwidth, 10 mV/cm	Waveform measurements and digital circuit analysis.
S1350	Wattmeter	2 and 10 watt ranges, terminating type.	Transmitter power output measurement.
S1067	Audio Oscillator	--	Audio signal measurements.
SLN6225	Isolation Transformer	1:1 turns ratio	Audio signal measurements.
R1013	SINAD Meter	40 mV to 10 V rms input	Receiver sensitivity measurements.
S1357	Frequency Counter	1 Hz resolution	Frequency measurements.

Table 6. Special Service Aids

MOTOROLA NUMBER AND ITEM DESCRIPTION	USE
ST1175 Dummy Battery Block	Interconnects unit to bench 7.5 V power supply.
NKN6222A Tune-Up Cable	Connects test equipment to the antenna jack on the radio section.
S1349A MX300 Portable Test Set or RTX4005A Portable Test Set and RTK4002 Test Cable	Enables convenient connections to the accessory jack, with switching functions.
ST1176 Battery Charger Tester	Permits rapidly checking the significant charger parameters.
ST1177 Battery Tester	Checking the batteries.
ST1178 Microphone Tester Adapter	Permits connecting the NMN6070 or NMN6071 external speaker-microphone to the ST855 microphone tester.
ST1179 Module Pusher	To push module guide pins for easy extraction without damage.
ST1180 RF Jack Wrench/Preselector Spanner Wrench	To remove the antenna jack and the nuts securing the preselector to the printed circuit board.
6682186E01 Tuning Tool	For adjusting the channel elements and the preselector.
Z2ETS-A Test Fixture (with special diagnostic EPROMs)	Needed for troubleshooting processor and interface boards in data processing portion of terminal.
NLN7219A or NLN4992A Processor Board and NLN7218A or NLN4995A Interface Board	Spare boards (known to be good) needed for troubleshooting data processing portion of terminal.
ST1091 Vacuum Desoldering Tool	Component removal.
ST909 IC Extractor	Dual in-line IC removal.
ST1190 "Dip Clip"	Permits attachment of test probes to dual in-line packages (DIPs).

Remote sensing leads are provided for external power supplies capable of remote voltage sensing, such as the Model S1348. Remote sensing will compensate for any voltage drop between the external power supply and the radio.

5. SKN6028 OR NKN6222 TUNE-UP CABLE

This 12-inch cable contains a connector that mates with the antenna jack on the unit. The cable is designed to interconnect the unit with 50-ohm RF test equipment such as a wattmeter or signal generator, with the BNC connector on the cable. The cable loss is 0.25 dB per foot.

6. S1349A PORTABLE TEST SET

The terminals have an accessory connector on the side of the housing. This connector contains several inputs and outputs to the unit, including an external microphone input to the IDC circuit, an external push-to-talk contact for keying the transmitter, the receiver discriminator output, and audio inputs and outputs to the final audio amplifier. The S1349 Portable Test Set attaches to the accessory connector and permits injecting inputs or monitoring outputs to troubleshoot the unit. The test set provides a convenient place to attach other test equipment and allows the technician to perform the following basic service operations.

a. Key the transmitter; either momentarily or continuously.

b. Modulate the transmitter; via an external audio oscillator for setting and measuring transmitter deviation.

c. Measure the modulation input voltage; to adjust transmitter deviation and measure modulation sensitivity.

d. Measure the internal microphone output; to check the microphone.

e. Measure receiver audio output; for aligning the receiver, checking receiver sensitivity, and measuring rated audio output. The test set contains an isolation transformer for properly connecting to the balanced audio output.

f. Measure discriminator ac voltage; for troubleshooting.

g. Measure discriminator dc voltage.

h. Measure ac output from the audio filter and regulator module U7.

i. Inject audio into audio power amplifier module U8; for troubleshooting.

RADIO ALIGNMENT PROCEDURES

1. GENERAL

The radio section is aligned at the factory to provide peak performance over a long period of time. Realignment may be required if components are replaced or have aged. To perform these procedures it is only necessary to remove the terminal section and back cover of the unit, as described in the "Disassembly Procedures."

Refer to the radio circuit board layout diagram (Figure 51) for the locations of adjustments.

2. RECEIVER ALIGNMENT

Preliminary Adjustments

1. Set squelch control to maximum ccw position (if applicable).
2. Set frequency select switch to F1 position on 2-channel models (N1258A).
3. Turn Z1 thru Z7 until they are flush with the circuit board.

STEP	ADJUST	FOR	MEASURED AT	USING	NOTE
1	Z6 & Z7	Maximum VDC (approximately 0.7 V)	M2	DC voltmeter (DC multimeter)	See Preliminary Adjustments
2	Freq dial on service monitor	Carrier freq of F1 (minus 21.4 MHz)	Pin 7 of preselector	Service monitor	Connect a Motorola TEK-10 probe to the PRESELECTOR input on the service monitor
3	CE1	Zero error	Pin 7 of preselector	Freq meter on service monitor	Freq select switch (FS) set at F1
4	Repeat steps 2 and 3 for second channel in the radio, if applicable (CE2/F2).				
5	Z1 thru Z5	Best quieting (lowest ac voltage) with freq select switch set to channel used in step 1	J402, pin 10 to pin 2 (Accessory connector)	AC voltmeter with 1:1 isolation transformer	Inject carrier freq at J401 to produce 20 dB quieting. While tuning Z1 thru Z5, adjust the input to maintain 20 dB quieting.
20 dB QUIETING TEST (Perform on each channel)					
1	Volume Control	1.73 VAC noise out	J402, pin 10 to pin 2	AC voltmeter with 1:1 isolation transformer	Establishes reference noise level for no signal input
2	Signal generator	Carrier freq, 0 output level	Generator output connector	Signal generator on service monitor	Connect signal generator to J401 (External Antenna Jack)
3	Signal generator output level	Slowly increase until noise decreases 20 dB	J402, pin 10 to pin 2	AC voltmeter with 1:1 isolation transformer	Signal must be less than 0.5 uV at J401 for 20 dB quieting

NOTE: Channel element (CE1, CE2) frequency = $(f_c - 21.4\ \text{MHz}) / 6$

3. TRANSMITTER ALIGNMENT

NOTES:

1. Align the receiver before adjusting channel elements CE101 or CE102.
2. Measurements are made with transmitter keyed and a 50-ohm load connected at J401.*
3. Frequency select switch (FS) used only on Model N1258A.

STEP	ADJUST	TEST EQUIPMENT USED		MEASUREMENT	
		TYPE	CONNECTED AT	CONDITIONS	DESCRIPTION & LEVEL
1	R107	Wattmeter	J401	Set frequency select switch (FS) to lowest power channel (if applicable)	2 W
		Ammeter (DC Multimeter)	DC supply		1225 mA
2	CE101	Frequency meter (on service monitor)	Radiated	FS set to position using CE101 (if applicable)	Transmit carrier frequency
3	CE102	Frequency meter (on service monitor)	Radiated	FS set to position using CE102 (if applicable)	Transmit carrier frequency
4	R102	Deviation meter (on service monitor)	Radiated	FS set to the channel having the highest deviation	± 5 kHz max. carrier dev
		Audio oscillator	J402, pin 3	Set to 1 kHz, 0.025 V	
5	none	Deviation meter (on service monitor)	Radiated	FS set to the channel having the highest deviation	

* Add a temporary jumper wire between points I9 and I10 at the end of the Interconnect Flex Circuit (Figure 48). Be sure to remove this jumper after transmitter alignment is complete.

TROUBLESHOOTING

1. GENERAL

The data terminal is designed for high reliability and for rapid service when trouble does occur. The best troubleshooting aid is a thorough understanding of the unit and the function of each module. The plug-in modular construction in the radio section eliminates the laborious, time consuming, troubleshooting procedures previously required to find a defect. Since the plug-in modules can be rapidly replaced, the following procedures are provided to help quickly isolate troubles to a defective stage.

2. RADIO SERVICE NOTES

a. The main printed circuit board is a 4-layer board with two layers of printed circuit bonded inside the board.

b. Before removing the 4-layer board from the frame, unsolder the B+, B-, wires connecting the antenna jack to the board, and the ground wire at the bottom of the board.

c. The audio output to the speaker is a balanced output. Do not measure with a grounded voltmeter. Use a battery powered voltmeter or a 1:1 transformer, such as the Motorola Part No. 2584903H01. This transformer has two secondary windings which must be connected in series to provide 1:1 turns ratio.

d. Flexible printed circuits are used in this radio. The foil pattern is bonded between two layers of flexible material. Use care when handling, avoid excessive bending. Do not overheat.

CAUTION

Use a temperature-controlled soldering iron with a 600°F or 700°F tip. Avoid prolonged contact with the flexible circuit.

e. To connect the radio to a 7.5-volt bench power supply, use battery block ST1175 and a current limiting power supply set at 3 amp maximum.

f. FCC regulations state that:

(1) Radio transmitters may be tuned or adjusted only by persons holding a first or second class commerical radiotelephone operator's license or by personnel working under their immediate supervision.

(2) The RF power output of a radio transmitter shall be no more than that required for satisfactory technical operation considering the area to be covered and the local conditions.

(3) Frequency and deviation of a transmitter must be checked before it is placed in service and rechecked once each year thereafter.

3. RADIO MODULE REMOVAL INSTRUCTIONS

Module locations are shown in Figure 23. Use the module pusher tool and remove modules with care as follows:

MODULE	REMOVAL PROCEDURE
Preselector and Transmitter Filter U107	Remove the threaded nuts securing the module to the board. Then press on the threaded studs and pull the module straight out from the component side.
Channel Elements	Push on the guide pin and the warp-coil-form from the solder side of the board using Module Pusher ST 1179. Then grasp the module with seizers and pull straight out from the component side.
U105	Grasp the module with seizers and pull straight out.
All other modules	Push on the guide pins from the solder side of the board using the Module Pusher ST 1179. Then grasp the module with seizers and pull straight out from the component side.

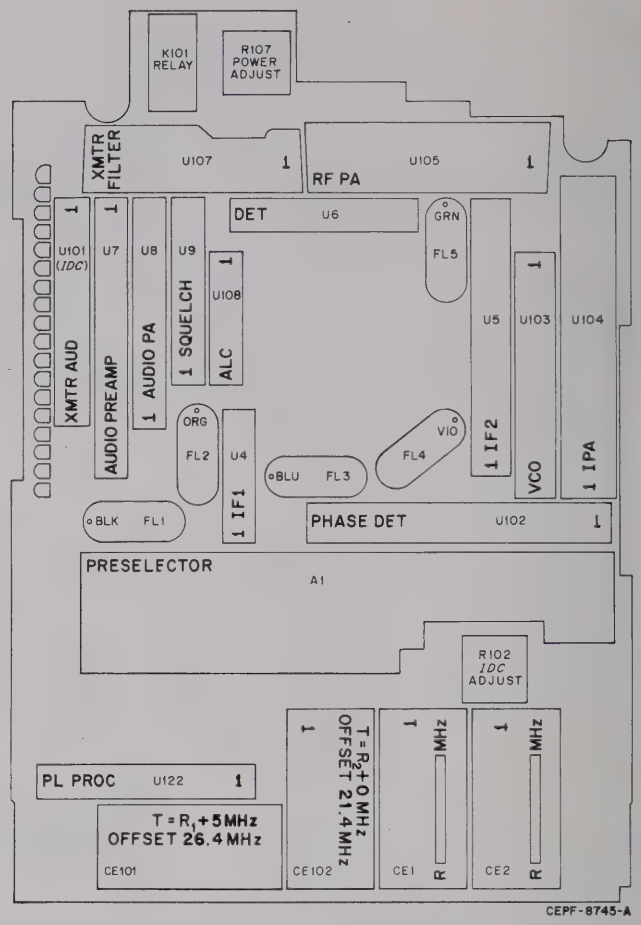


Figure 23. Radio Module Locations

4. ACCESSORY CONNECTOR

The accessory connector pins provide several signal outputs and also provide points for injecting signals. The Motorola S1349 or RTX4005A MX300 Portable Test Set uses this capability for rapid troubleshooting. Refer to the accessory connector troubleshooting diagram (Figure 24) for information on each pin of the connector.

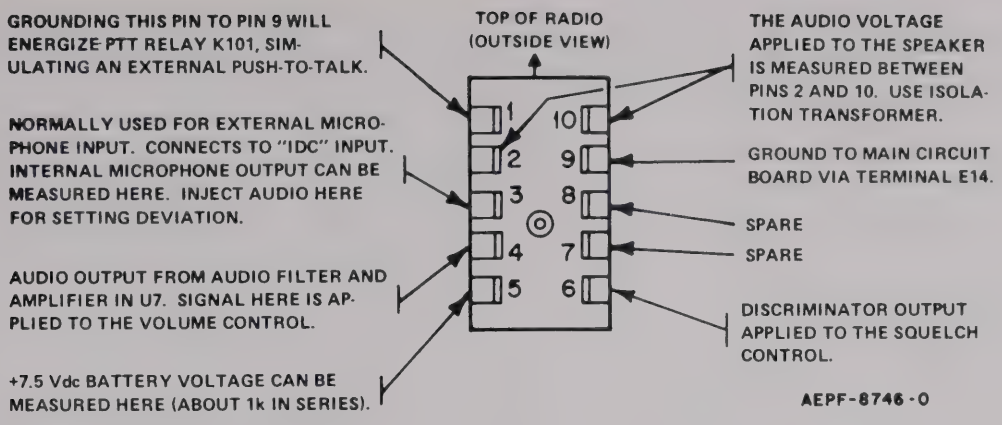

GROUNDING THIS PIN TO PIN 9 WILL ENERGIZE PTT RELAY K101, SIMULATING AN EXTERNAL PUSH-TO-TALK.
NORMALLY USED FOR EXTERNAL MICROPHONE INPUT. CONNECTS TO "IDC" INPUT. INTERNAL MICROPHONE OUTPUT CAN BE MEASURED HERE. INJECT AUDIO HERE FOR SETTING DEVIATION.
AUDIO OUTPUT FROM AUDIO FILTER AND AMPLIFIER IN U7. SIGNAL HERE IS APPLIED TO THE VOLUME CONTROL.
+7.5 Vdc BATTERY VOLTAGE CAN BE MEASURED HERE (ABOUT 1k IN SERIES).
TOP OF RADIO (OUTSIDE VIEW)
1
2
3
4
5
6
7
8
9
10
THE AUDIO VOLTAGE APPLIED TO THE SPEAKER IS MEASURED BETWEEN PINS 2 AND 10. USE ISOLATION TRANSFORMER.
GROUND TO MAIN CIRCUIT BOARD VIA TERMINAL E14.
SPARE
SPARE
DISCRIMINATOR OUTPUT APPLIED TO THE SQUELCH CONTROL.
AEPF-8746-0

Figure 24.
Accessory Connector Troubleshooting Diagram

5. RADIO PERFORMANCE CHECKS USING THE S1349A PORTABLE TEST SET

a. Receiver Alignment Applications

(1) Connect the test set to the accessory connector on the side of the radio.

(2) Connect an ac voltmeter to the audio out and dc metering jack on the test set.

(3) Set the test set controls as follows:

(a) Input Selector - Any position

(b) Speaker Switch - On or off position

(c) Metering Switch - Audio PA out position

(d) PTT Switch - Unkeyed center position

(4) The receiver audio output is now connected to the ac voltmeter through an isolation transformer. This provides a convenient method of making quieting checks and adjustments. Refer to the alignment procedure (paragraph 3b).

b. Typical Performance Checks

Several circuits in the radio can be quickly checked for overall performance using the test set. Table 7 lists several checks that will quickly isolate faulty performance to a functional circuit.

(1) Connect the test set to the accessory connector on the side of the radio.

(2) Connect an ac voltmeter or audio oscillator to the test set as instructed in Table 7. A wattmeter or dummy load should be connected at the antenna jack on the radio when checking transmitter operation.

(3) Refer to the other columns in Table 7 for test set control settings and interpretation.

6. RADIO RECEIVER TROUBLESHOOTING

a. Preselector Troubleshooting

Refer to the troubleshooting diagram of the preselector circuit; Figure 25.

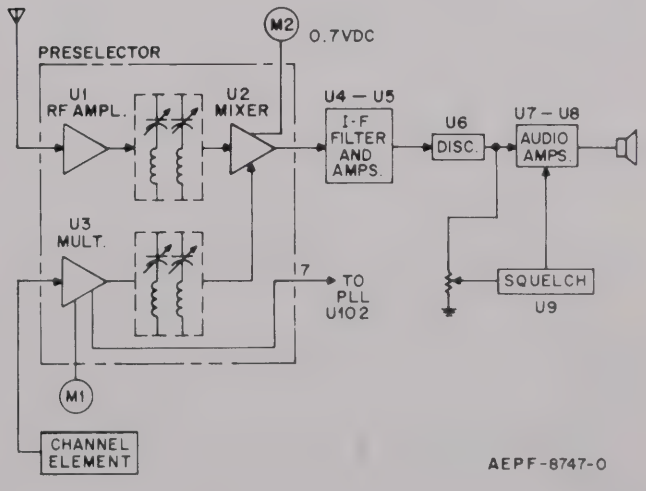


Figure 25. Preselector Circuits, Troubleshooting Diagram

Table 7. Performance Check Chart Using the S1349 Test Set

FUNCTION BEING CHECKED	TEST EQUIPMENT CONNECTIONS	TEST SET CONTROL SETTING				COMMENTS
		Input Selector	PTT Switch	Speaker Switch	Metering Switch	
RECEIVER SENSITIVITY	AC voltmeter to "Audio out and DC metering" jack	Any Position	Unkeyed Center Position	"ON" or "OFF"	"Audio PA Out"	Under these conditions, the receiver audio output is connected to the AC voltmeter through an isolation transformer. Proceed with 20 dB quieting check.
RECEIVER AUDIO OUTPUT	AC voltmeter to "Audio out and DC metering" jack	Any Position	Unkeyed Center Position	"ON" or "OFF"	"Audio PA Out"	With an "ON" carrier 100 uV signal applied to the radio, modulated with a 1000 Hz tone @±5 kHz, and the volume control set at maximum, the AC voltmeter should read no less than 3.74 VAC.
TRANSMITTER FREQUENCY & POWER OUTPUT	None to Test Set	Any Position	Keyed UP or DOWN	"ON" or "OFF"	Either Position	The test set provides a means of keying the transmitter for tests. Frequency error and power output can now be noted.
TRANSMITTER DEVIATION ADJUSTMENT	Audio oscillator to "Audio in" jack. AC voltmeter to "Audio out and DC metering" jack.	"Mic"	Keyed UP or DOWN	"ON" or "OFF"	"Audio In/Out"	Adjust audio oscillator input for 25 mV @ 1000 Hz. Adjust IDC for ±5 kHz deviation.
TRANSMITTER MODULATION SENSITIVITY	Audio oscillator to "Audio in" jack. AC voltmeter to "Audio out and DC metering" jack.	"Mic"	Keyed UP or DOWN	"ON" or "OFF"	"Audio In/Out"	Adjust audio oscillator for 3.5 mV @ 1000 Hz. With PL tone filter removed, deviation should be no less than ±3 kHz.
DISCRIMINATOR OUTPUT	DC and AC voltmeter to "Audio out and DC metering" jack. (See comment column)	"Disc"	Unkeyed Center Position	"ON"	"Audio In/Out"	Noise should be heard from speaker. AC voltmeter should indicate 250 to 400 mV of noise, or recovered audio if 100 uV fc is applied with 1000 Hz tone @ ±5 kHz. NOTE: With no carrier applied, 1.3 to 1.8 VDC will be present at the "Audio out and DC metering" jack.
OUTPUT OF AUDIO FILTER & REGULATOR MODULE U7	AC voltmeter to "Audio out and DC metering" jack.	"Volume Control"	Unkeyed Center Position	"ON" or "OFF	"Audio In/Out"	Apply an on carrier signal at 100 uV, modulated with 1000 Hz tone @±3 kHz. The AC voltmeter should indicate an output of more than 62 mVAC.
INJECT AUDIO INTO AUDIO POWER AMP	Audio oscillator to "Audio in" jack. Output set at 1000 Hz.	"Volume Control"	Unkeyed Center Position	"ON" or "OFF"	"Audio In/Out" for input. Audio PA out" for output	Inject 325 mV of 1000 Hz. By adjusting the volume control, full audio output (3.74 VAC) should be available at output.
OUTPUT OF MICROPHONE	AC voltmeter to "Audio out and DC metering" jack.	"Mic"	Unkeyed Center Position	"ON" or "OFF"	"Audio In/Out"	Key transmitter with PTT switch on radio. AC voltmeter is indicating output of microphone. A loud whistle or "four" into the microphone should cause an ACVM reading of 25 mV or greater.

A change in the dc voltage at test point M2 in the preselector is an indication of injection. The dc voltage reading at M2 should decrease by approximately 0.25 V dc when the channel element output is shorted to ground using a .001 uF capacitor.

The receiver injection frequency can be checked at pin 7 of the preselector to insure multiplier operation. The frequency out of the multipliers is 21.4 MHz below carrier frequency. A properly operating preselector will read a peak dc voltage of about 0.7 V dc at M2.

b. I-F And Audio Circuits

The i-f circuit consists of modules U4, U5, and crystal filters FL1 through FL5. The idealized gain of U4 and U5 combined is over 135 dB. Because of this high gain, the possibility of oscil-

lation exists when test equipment is connected to pins on the modules. With a 21.4 MHz i-f input signal present, and with oscillation occurring, you cannot tell which signal is being measured. This can lead you to believe that the input signal is being amplified when, in fact, you are measuring the self-sustained oscillation caused by connecting the test equipment. To avoid this condition, remove module U5 when making measurements around U4.

Making RF measurements at U4 is affected by other factors. The crystal filters present a source impedance to U4 of about 1 k at the i-f frequency of 21.4 MHz. The input capacitance of your test equipment (if larger than 10 pF) will present some reactance at 21.4 MHz and load the circuit enough to cause erroneous readings – in addition to possible oscillation.

If trouble is suspected in U4 or U5, replace the suspected module with a known good module. If new modules do not solve the problem, replace the crystal filters.

NOTE

Crystal filters FL1/FL2 and FL3/FL4 are matched pairs. Refer to the parts list and always replace both filters of a pair when necessary.

Receiver noise levels are a valuable troubleshooting aid. These noise levels will change should a problem occur in the receiver. By knowing the normal and abnormal levels at key points in the receiver, you can quickly isolate a receiver problem.

The following chart (Table 8) lists the normal and abnormal noise levels at both the discriminator output (pin 6 of J402) and audio output (to the speaker). The readings are taken with a standard ac voltmeter connected to the S1349A Test Set.

Table 8. Typical I-F and Audio Circuit Voltages

CONDITION	VOLTAGE MEASUREMENT	
	DISCR OUTPUT PIN 6 OF J402	AUDIO OUTPUT USING TEST SET
Normal	250-400 mV ac	4.5 V ac
U4 failed	10-40 mV ac	150-300 mV ac
U5 failed	less than 10 mV ac	less than 10 mV ac
U6 failed	less than 10 mV ac	less than 10 mV ac
U7 failed	less than 15 mV ac	0 V
U8 failed	250-400 mV ac	0 V

The chart does not cover all possible failure modes; however, it will aid in troubleshooting most receiver problems.

c. Squelch Circuit

Refer to the squelch circuit troubleshooting diagram in Figure 26.

Approximately 30 mV of noise is required at pin 6 of U9, the squelch module, for squelch action. With the proper input at pin 6 of U9, the output at pin 4 should be 4 V dc, turning off the audio stages. The dc voltage reading at pin 4 of U9 should also change from 0 V dc to 4 V dc as the squelch control is rotated clockwise.

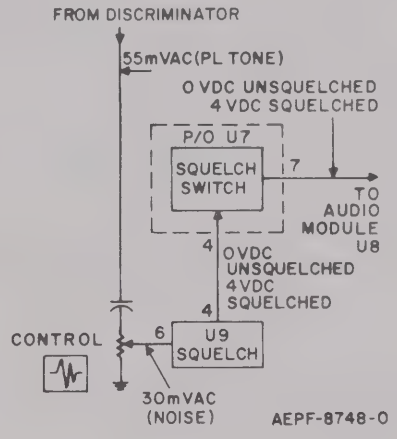


Figure 26.
Squelch Circuit Troubleshooting Diagram

7. RADIO TRANSMITTER TROUBLESHOOTING

a. Transmitter Current Analysis

Since transmitter currents are relatively large, monitoring the 7.5-volt power supply current provides a quick analysis of overall transmitter operation. This is especially true with the RF power amplifier modules, which require 350 mA or more when operating normally.

With a wattmeter or dummy load connected at the antenna jack, key the transmitter and observe the total current supplied to the radio. Refer to Table 9 for possible defective modules.

Table 9.
Transmitter Troubleshooting by Current Measurement

TOTAL CURRENT (mA)	ANALYSIS
Less than 200	There is probably no VCO output and power amplifiers U104 and U105 are turned off. Suspect a defective channel element, U102, or U103.
200	U104 is not turned on, which keeps U105 turned off, even though there is a VCO output. Suspect defective U104, U107, or U108.
575	U104 is turned on, meaning that VCO output is present and ALC circuit is working. Suspect defective U105.
1225	This is normal current for the transmitter. Since U107 contains a passive filter, suspect U107, or RF jack J401 if power output is not present.
NOTE: Current readings are nominal and may vary slightly. Relay K101 draws about 40 mA, LED CR303 draws about 15 mA, IDC module U101 draws about 10 mA, channel elements take about 6.0 mA, and VCO U103 about 70 mA. PLL Processor U102 draws about 70 mA.	

b. Phase-Locked Loop and VCO Circuits

The phase-locked-loop (PLL) circuit uses two modules to generate the transmitted carrier frequency. Phase-lock-loop processor module U102 and VCO module U103 operate in a closed loop, with an output from U102 driving U103, and an output from U103 fed back to U102. Due to signal levels and loading between the two modules, there is no convenient way to determine which of the two modules has failed when trouble is experienced in this circuit.

There are two conditions that occur during operation; search and lock. Search begins when the transmitter is keyed, and lock occurs almost instantly if the circuit is operating properly.

To determine if the VCO is locked on frequency or in the search condition, refer to the PLL and VCO troubleshooting diagram in Figure 27 and monitor the signal at pin 1 of U103 (input to the VCO). This signal will be a triangular waveform at about 4 volts p-p if there is a problem and the VCO is NOT LOCKED on frequency. If the sawtooth voltage is present, if the channel element frequency is present to U102, and if dc operating voltages are present, then U102 or U103 is probably defective. Since U102 contains the most circuitry, try substituting this module first. If the triangular voltage is still present, replace module U103. If lock is present, the dc voltages in the diagram should be measured.

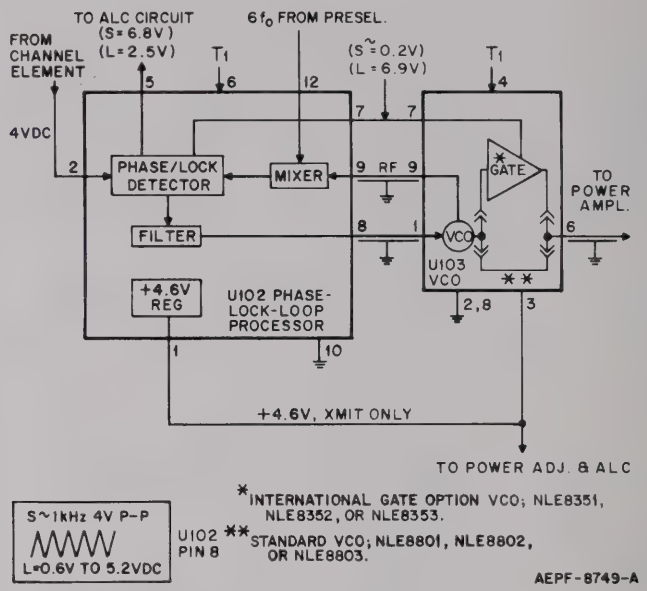


Figure 27. PLL Troubleshooting Diagram

NOTE

If the VCO is not locked on frequency, the RF amplifiers will be turned off and total transmitter current will be around 200 mA or less.

c. Radio Circuit Board Troubleshooting

The radio circuit board (four-layer board) contains two internal layers that are not accessible or visible. Point-to-point circuit tracing is not difficult since all module pins are available from the back side of the board.

Signal paths are usually from the output of one module to the input of the next module and are easily followed with the radio schematic diagram (Figure 50) and the circuit board (Figure 51).

8. DATA TERMINAL TROUBLESHOOTING

This section describes troubleshooting techniques used to localize faults relating to the interface and processor boards in the data terminal portion of the unit. The best troubleshooting aid is a thorough understanding of the unit and the functions performed by each of the two data processing boards, as given in the Theory of Operation section of this manual. The troubleshooting procedures given here are presented in the form of a series of flow charts which isolate problems down to the integrated circuit package and component levels. Additional servicing must be handled by the Motorola National Data Services group.

Motorola National Data Services support activities are centered in two principal locations: Schaumburg, Illinois and Phoenix, Arizona. Refer to the Replacement Parts Ordering page at the back of this manual for addresses and telephone numbers.

a. General Overall Troubleshooting Chart

The following list of symptoms and corresponding suggested remedies are keyed to the general overall troubleshooting flow chart shown in Figure 28.

SYMPTOM	REMEDY (Figure 28)
Display shows one of the numbers 0 through 5 across entire display.	Entry point A
Display shows one of the letters L, U, B, or C across entire display.	Entry point A
No display; unit does not come on (polling mode) when ON key is pressed.	Entry point B
Keyboard malfunction; not all keys operate.	Entry point C
Display shows missing segments, characters, or a character stuck in "on" position.	Entry point D
Unit does not transmit in voice channel, or transmits in data channel when using the PTT switch.	Entry point E
Unit does not transmit on data channel.	Entry point F
Unit does not receive.	Entry point G
Unit keys transmitter, but no data is sent.	Entry point H
Alert tone malfunction.	Entry point J
Data terminal activates while in voice channel.	Entry point K
Microphone does not mute during data transmission.	Entry point L
Unit is not squelched on data channel.	Entry point M

b. Interface Board Troubleshooting Procedures

The following procedures and corresponding suggested remedies are keyed to the detailed interface board troubleshooting flow charts shown in Figures 29 and 30.

(1) Preliminary Test Setup

- Install interface board to be tested in the Z2ETS-A Test Fixture (Table 6), along with the NLN7219A* or NLN4992A Processor Board (known to be good) and test interface cable (16-pin plug).
- Install diagnostic EPROMs in U919 and U920 position of processor board.
- Place S3 of fixture in test position (loopback mode).
- Place S18 of fixture in the "channel 1" position.

(2) Troubleshooting Procedures

Follow the troubleshooting test procedures until a failure mode is encountered; then proceed to the designated flow chart entry point.

PROCEDURE (Symptom)	REMEDY (Figures 29 and 30)
Blank display appears when test fixture is activated.	Entry point A
All 0's, 1's, 2's, or 3's appear across display.	Entry point J
"RAM TEST 60" display should appear. If segments or whole characters are missing then troubleshoot. This test only checks RAMs on processor board, therefore, if display is OK, abort to main diagnostic by pushing KEY A.	Entry point C
After 60-second RAM test or abort from RAM test, if "I" characters or the flag line format appear on display, troubleshoot.	Entry point B

*NLN7219A used to test boards with light pen option circuits.

PROCEDURE (Symptom)	REMEDY (Figures 29 and 30)
After 60-second RAM test or abort from RAM test, if "(UNIT ? -- <ØØØØ>)" display appears, but segments or whole characters are missing.	Entry point C
If display appears correctly (UNIT ? -- <ØØØØ>), enter unit ID number (1st two digits of code plug cap code). If ID does not appear, check flex cable.	Entry point H
Observe display; it should indicate H (or L) SYNC/PPPP.	Entry point D
Press ON key (or close S11 on fixture); all segments and all characters should appear on display.	Entry point C
Press period (.) key (or close S13 on fixture). All T characters should appear on display and tone heard from speaker.	Entry point E
Press Ø key (or close S12 on fixture). Keys transmitter and modulates via Q line.	Entry point F
Press SPACE key (or close S6 on fixture). Display shows flag line status. Lower supply voltage until flag line 4 shows character L (trip voltage is 6.0 to 6.5 V).	Entry point G
Press keys (ENT, →|, |←, A, B, C, D, H, S, BRT, 3, P, 6, 9, X. Observe column arrow and proper row number.	Entry point H

If the interface board contains the light pen option circuits, refer to paragraph d.

c. Processor Board Troubleshooting Procedures

The following procedures and corresponding suggested remedial steps are keyed to the detailed processor board troubleshooting flow charts given in Figures 31 and 32.

(1) Preliminary Test Setup

- Install processor board to be tested in the Z2ETS-A Test Fixture (Table 6), along with the NLN7218A* or NLN4995A Interface Board (known to be good) and test interface cable (16-pin plug).
- Place S3 of fixture in test position (loop-back mode).
- Apply power to fixture; if display shows any of the numerals Ø to 5 across the entire display, or if display remains blank after pressing the "on" key, proceed to entry point K in troubleshooting flow chart (Figure 31).

* NLN7218A used to test boards with light pen option circuits.

(2) Troubleshooting Procedures

Install diagnostic EPROMs in U919 and U920 positions of processor board. Follow the troubleshooting test procedures until a failure mode is encountered; then proceed to the designated flow chart entry point.

PROCEDURE (Symptom)	REMEDY (Figures 31 and 32)
Blank display appears when test fixture is activated (or random segments lighted).	Entry point L
All Ø's, 1's, 2's, or 3's appear across the display.	Entry point M
Letters L, U, B, or C appear across the display before entering RAM test.	Entry point N
NOTE "RAM TEST 60" display should appear. If segments or whole characters are missing, then troubleshoot.	Entry point R
Letters L, U, or B appear across display during RAM test.	Entry point N'
NOTE If processor board under test has already gone through the 60-second RAM test at least once and RAMs have not been changed, the RAM test may then be aborted to main diagnostic by actuating the A key.	
After RAM test, all I's appear across the display.	Entry point P
After RAM test, the flag line display appears, "EF3 FAILURE."	Entry point Q
After RAM test, if "UNIT? -- <ØØØØ>" display appears, but segments or characters are missing.	Entry point R
If display appears correctly (UNIT ? -- <ØØØØ>), enter unit ID number (1st two digits of code plug cap code). If ID does not appear, check flex cable.	Entry point S'
Observe display; it should indicate H (or L) SYNC/PPPP.	Entry point S
Press keys 2nd, A, D, and E; this checks the four input (I/O) lines. Observe column arrow and proper row number.	Entry point S'
Press ON key (or close S11 on fixture); all segments and all characters should appear on display.	Entry point R
Press period (.) key (or close S13 on fixture). All T characters should appear on display and tone heard from speaker.	Entry point T

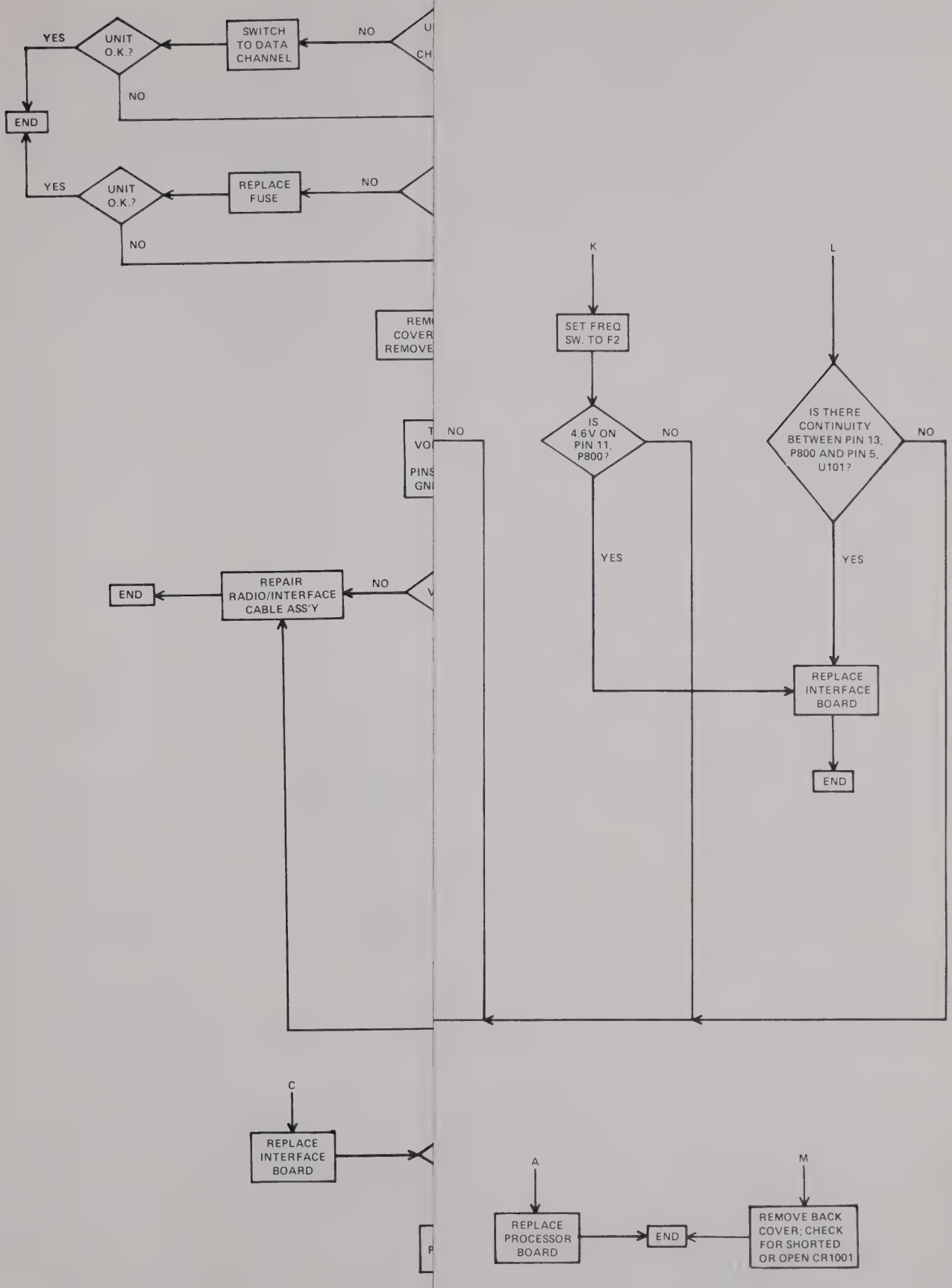


Figure 28. General Overall Troubleshooting Flow Chart

PROCEDURE (Symptom)	REMEDY (Figures 29 and 30)
After 60-second RAM test or abort from RAM test, if "(UNIT ? -- < ØØØØ >)" display appears, but segments or whole characters are missing.	Entry point C
If display appears correctly (UNIT ? -- < ØØØØ >), enter unit ID number (1st two digits of code plug cap code). If ID does not appear, check flex cable.	Entry point H
Observe display; it should indicate H (or L) SYNC/PPPP.	Entry point D
Press ON key (or close S11 on fixture); all segments and all characters should appear on display.	Entry point C
Press period (.) key (or close S13 on fixture). All T characters should appear on display and tone heard from speaker.	Entry point E
Press Ø key (or close S12 on fixture). Keys transmitter and modulates via Q line.	Entry point F
Press SPACE key (or close S6 on fixture). Display shows flag line status. Lower supply voltage until flag line 4 shows character L (trip voltage is 6.0 to 6.5 V).	Entry point G
Press keys (ENT, →|, |←, A, B, C, D, H, S, BRT, 3, P, 6, 9, X. Observe column arrow and proper row number.	Entry point H

If the interface board contains the light pen option circuits, refer to paragraph d.

c. Processor Board Troubleshooting Procedures

The following procedures and corresponding suggested remedial steps are keyed to the detailed processor board troubleshooting flow charts given in Figures 31 and 32.

(1) Preliminary Test Setup

- Install processor board to be tested in the Z2ETS-A Test Fixture (Table 6), along with the NLN7218A* or NLN4995A Interface Board (known to be good) and test interface cable (16-pin plug).
- Place S3 of fixture in test position (loop-back mode).
- Apply power to fixture; if display shows any of the numerals Ø to 5 across the entire display, or if display remains blank after pressing the "on" key, proceed to entry point K in troubleshooting flow chart (Figure 31).

* NLN7218A used to test boards with light pen option circuits.

(2) Troubleshooting Procedures

Install diagnostic EPROMs in U919 and U920 positions of processor board. Follow the troubleshooting test procedures until a failure mode is encountered; then proceed to the designated flow chart entry point.

PROCEDURE (Symptom)	REMEDY (Figures 31 and 32)
Blank display appears when test fixture is activated (or random segments lighted).	Entry point L
All Ø's, 1's, 2's, or 3's appear across the display.	Entry point M
Letters L, U, B, or C appear across the display before entering RAM test.	Entry point N
NOTE "RAM TEST 60" display should appear. If segments or whole characters are missing, then troubleshoot.	Entry point R
Letters L, U, or B appear across display during RAM test.	Entry point N'
NOTE If processor board under test has already gone through the 60-second RAM test at least once and RAMs have not been changed, the RAM test may then be aborted to main diagnostic by actuating the A key.	
After RAM test, all I's appear across the display.	Entry point P
After RAM test, the flag line display appears, "EF3 FAILURE."	Entry point Q
After RAM test, if "UNIT? -- < ØØØØ >" display appears, but segments or characters are missing.	Entry point R
If display appears correctly (UNIT ? -- < ØØØØ >), enter unit ID number (1st two digits of code plug cap code). If ID does not appear, check flex cable.	Entry point S'
Observe display; it should indicate H (or L) SYNC/PPPP.	Entry point S
Press keys 2nd, A, D, and E; this checks the four input (I/O) lines. Observe column arrow and proper row number.	Entry point S'
Press ON key (or close S11 on fixture); all segments and all characters should appear on display.	Entry point R
Press period (.) key (or close S13 on fixture). All T characters should appear on display and tone heard from speaker.	Entry point T

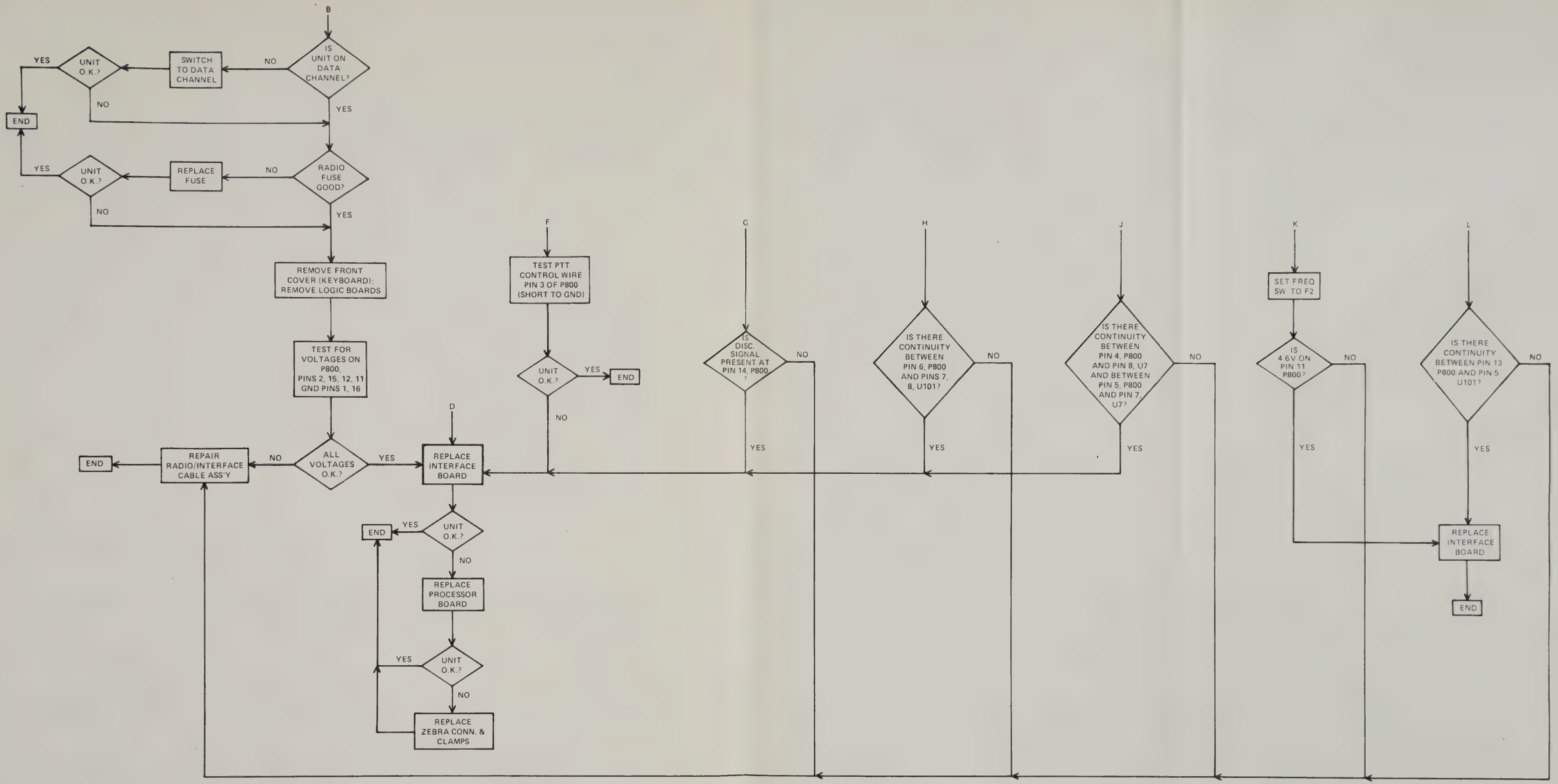


Figure 28. General Overall Troubleshooting Flow Chart

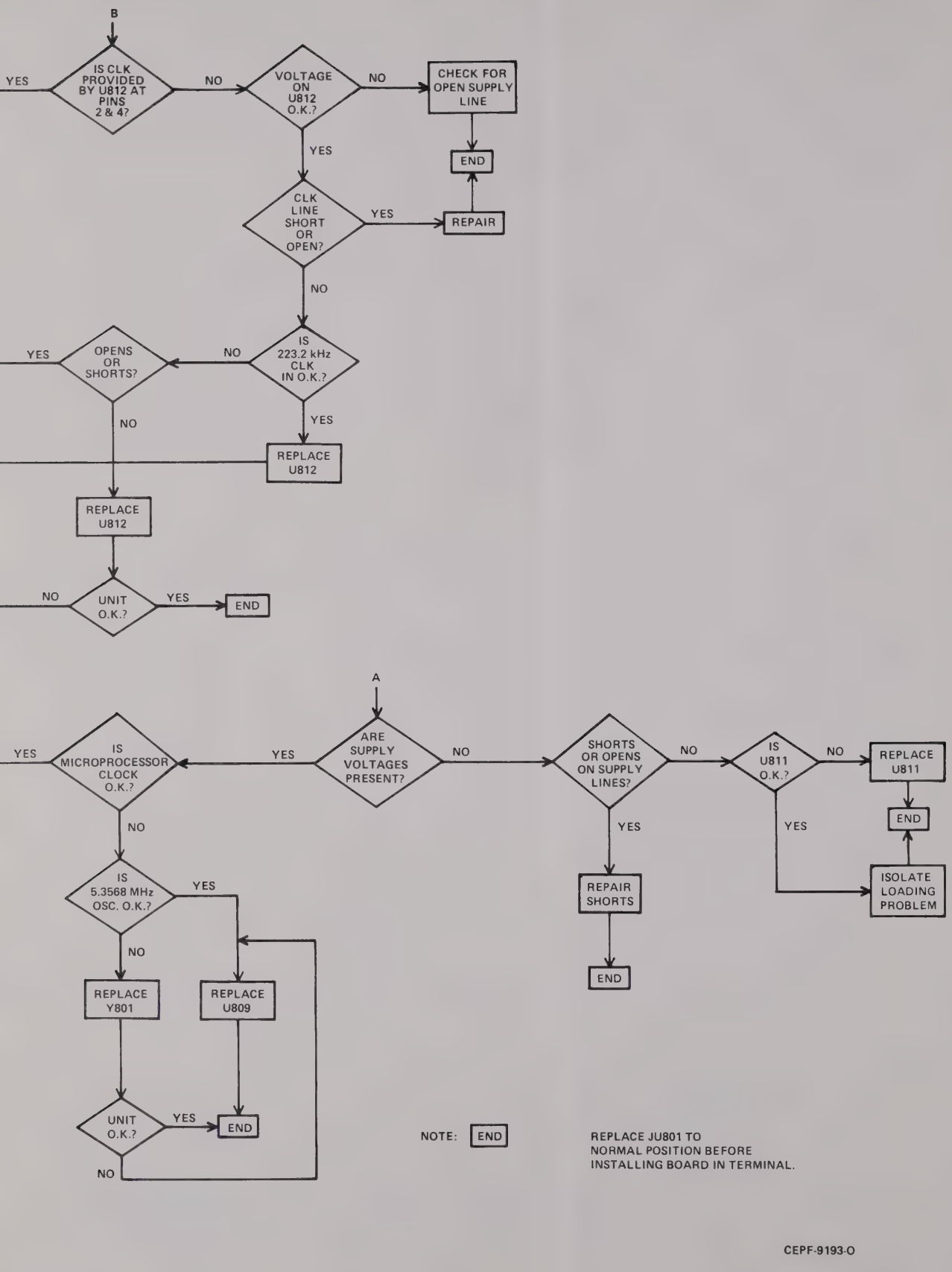


 Figure 29. Interface Board Troubleshooting Flow Chart (Part 1)

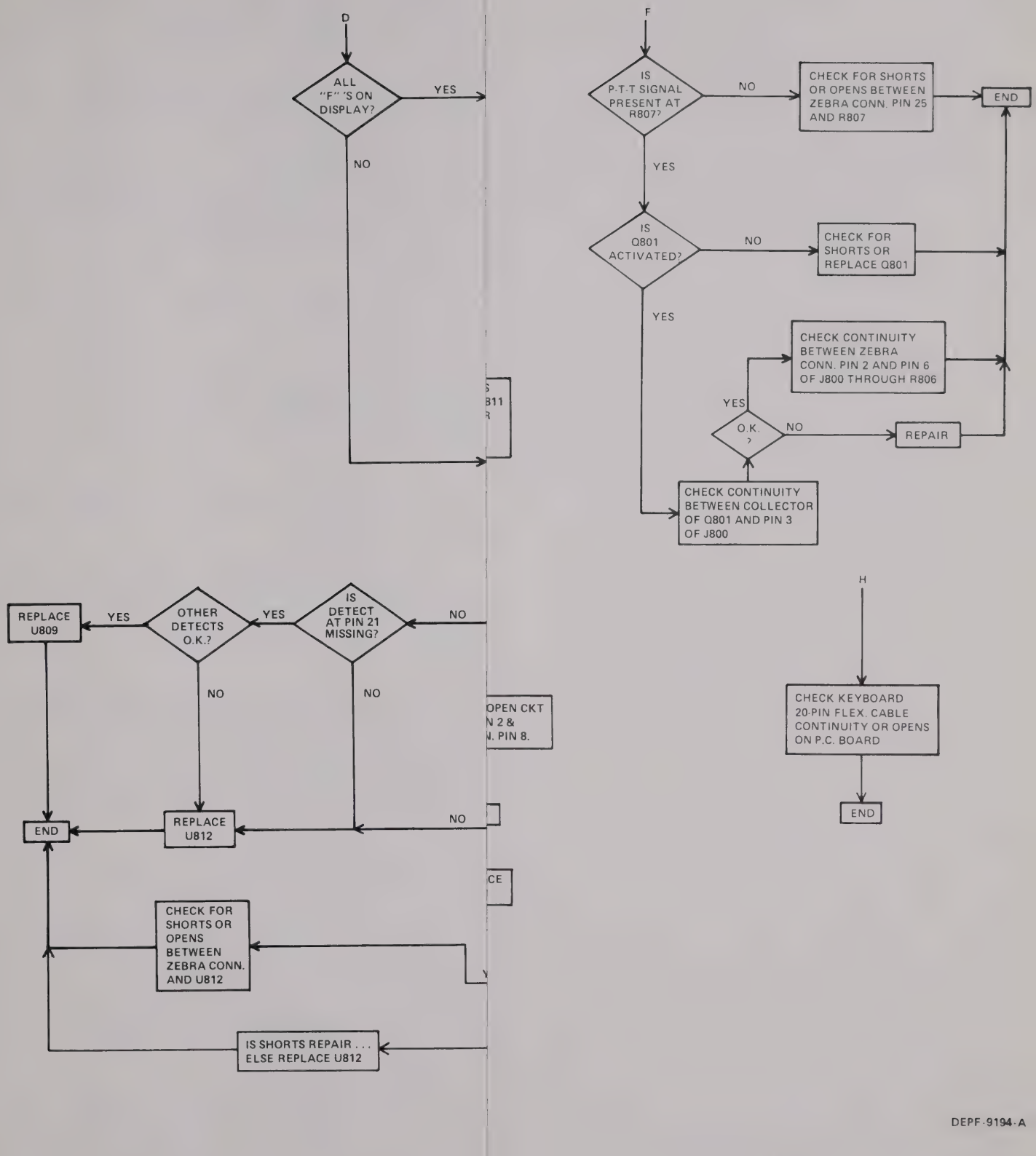


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Figure 30.
Interface Board Troubleshooting Flow Chart (Part 2)

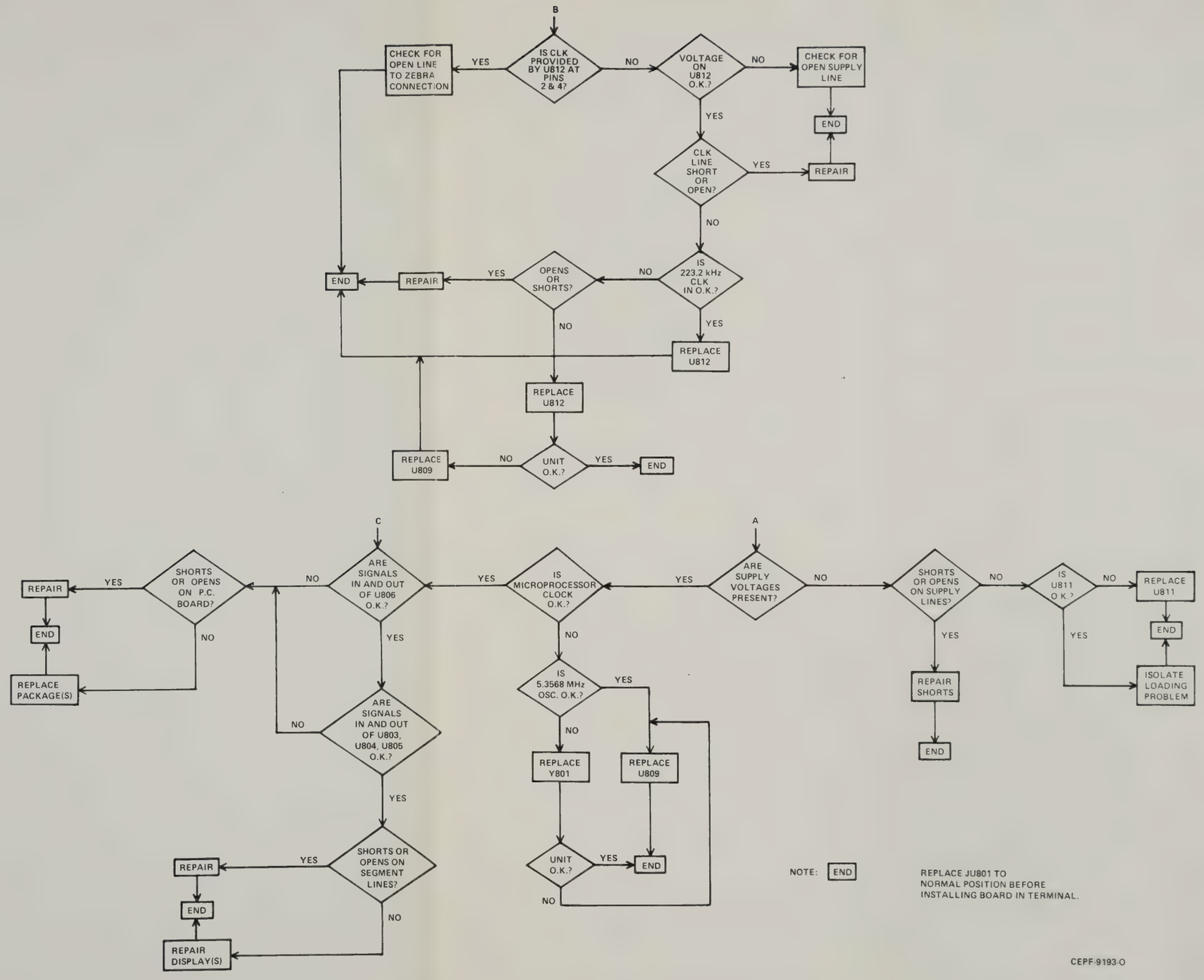

Figure 29. Interface Board Troubleshooting Flow Chart (Part 1)

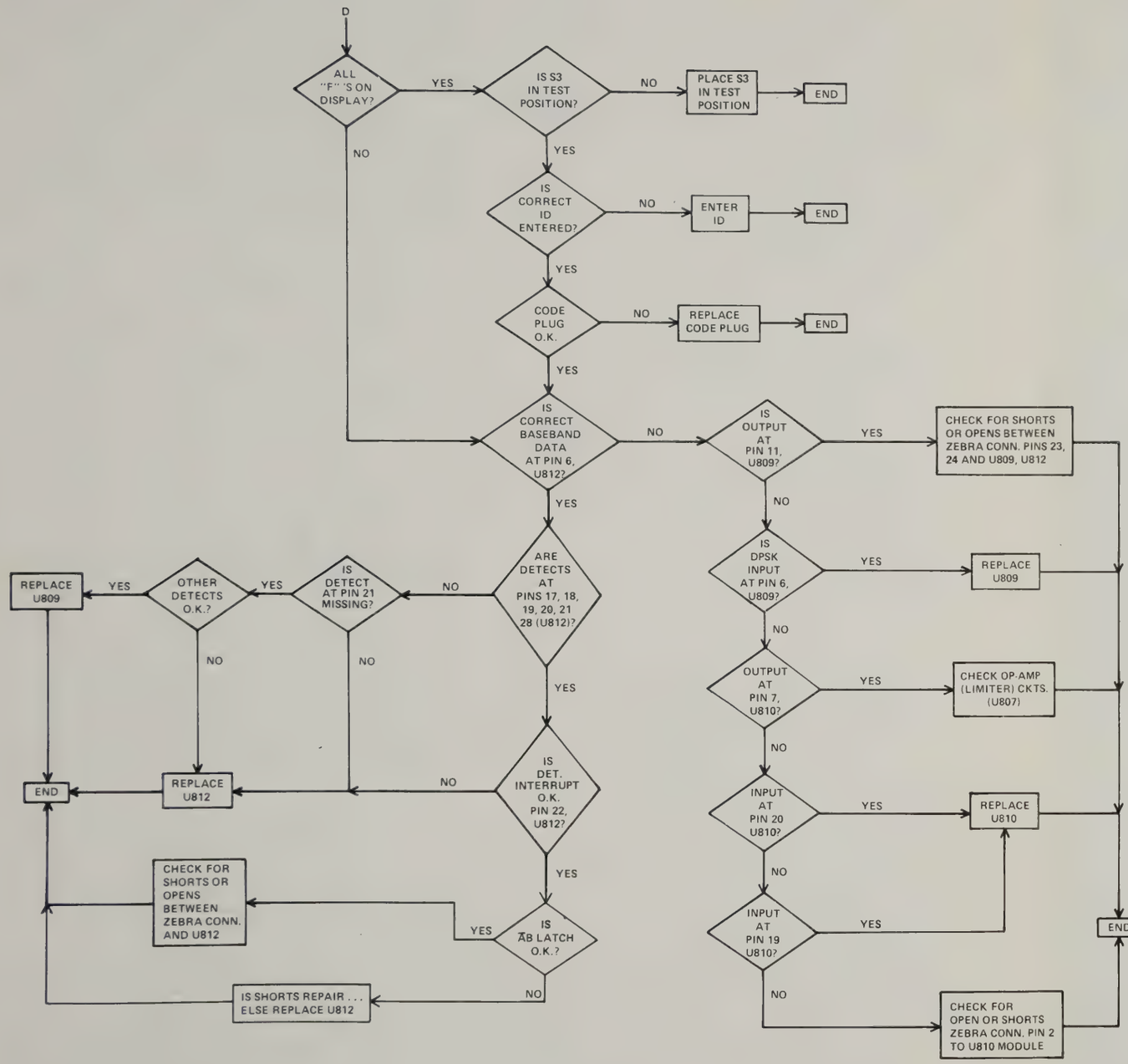

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Figure 30.
Interface Board Troubleshooting Flow Chart (Part 2)

PROCEDURE (Symptom)	REMEDY (Figures 31 and 32)
Press Ø key (or close S12 on fixture). Keys transmitter and modulates via Q line.	Entry point T
Press S key (or close S5 on fixture). Display is blanked and a low frequency tone is heard from speaker.	Entry point T
Press SPACE key (or close S6 on fixture). Display shows flag line inputs. Lower supply voltage until flag line 4 shows character L (trip voltage is 6.0 to 6.5 V).	Entry point U

NOTE

Complete the following procedures only if the processor board under test contains optional light pen circuitry.

PROCEDURE (Symptom)	REMEDY (Figure 32)
Reset power (enter 60-second RAM test) actuate the L key to enter the Light Pen home position. Observe the "LP TEST NO" on display. Using an oscilloscope, probe pins 4 and 7 of U902. Observe 3 μs pulses at an approximate repetition rate of 600 μs.	Entry point V
Pulses should be >5 V in amplitude.	Entry point W
Using an oscilloscope, probe cathodes of CR902 and CR903 and observe stretched pulses. The pulses should be between 80 μs and 160 μs wide at the +3 Vdc level.	Entry point X
Observe "LP PWR" lamp switching on and off with each push of the P key. Observe "2/3 RATIO" lamp switching on and off with each push of the R key.	Entry point Y
From home position, push the "5" key to enter the sample/hold leakage test. Observe the "POS S/H L?" display. Verify that the "S/H" lamp is on. Push the L key, "S/H" lamp should go off and the prompt will reappear in ≃10 seconds after alert is sounded. Push key "H" to return to home position.	Entry point Z

d. Light Pen Circuits Troubleshooting Procedures

Before troubleshooting the light pen circuits, you must complete the preliminary processor and interface board tests outlined in preceding paragraphs 8.b. and 8.c. The following tests relate only to the NKN6259A light pen connector board and the NLN7218A interface board with light pen circuitry. Tests concerning the NLN7219A processor board with light pen circuits are contained in paragraph c.

(1) General Overall Troubleshooting Chart

PROCEDURE (Symptom)	REMEDY (Figure 33)
Unit does not detect white (display does not blank when light pen is placed on white surface).	Entry point A
Light pen detects white but does not enter data (with beep alert tone) when code is scanned.	Entry point B
Unit always gives error indication (one beep alert tone followed by three beep alert tones).	Entry point C

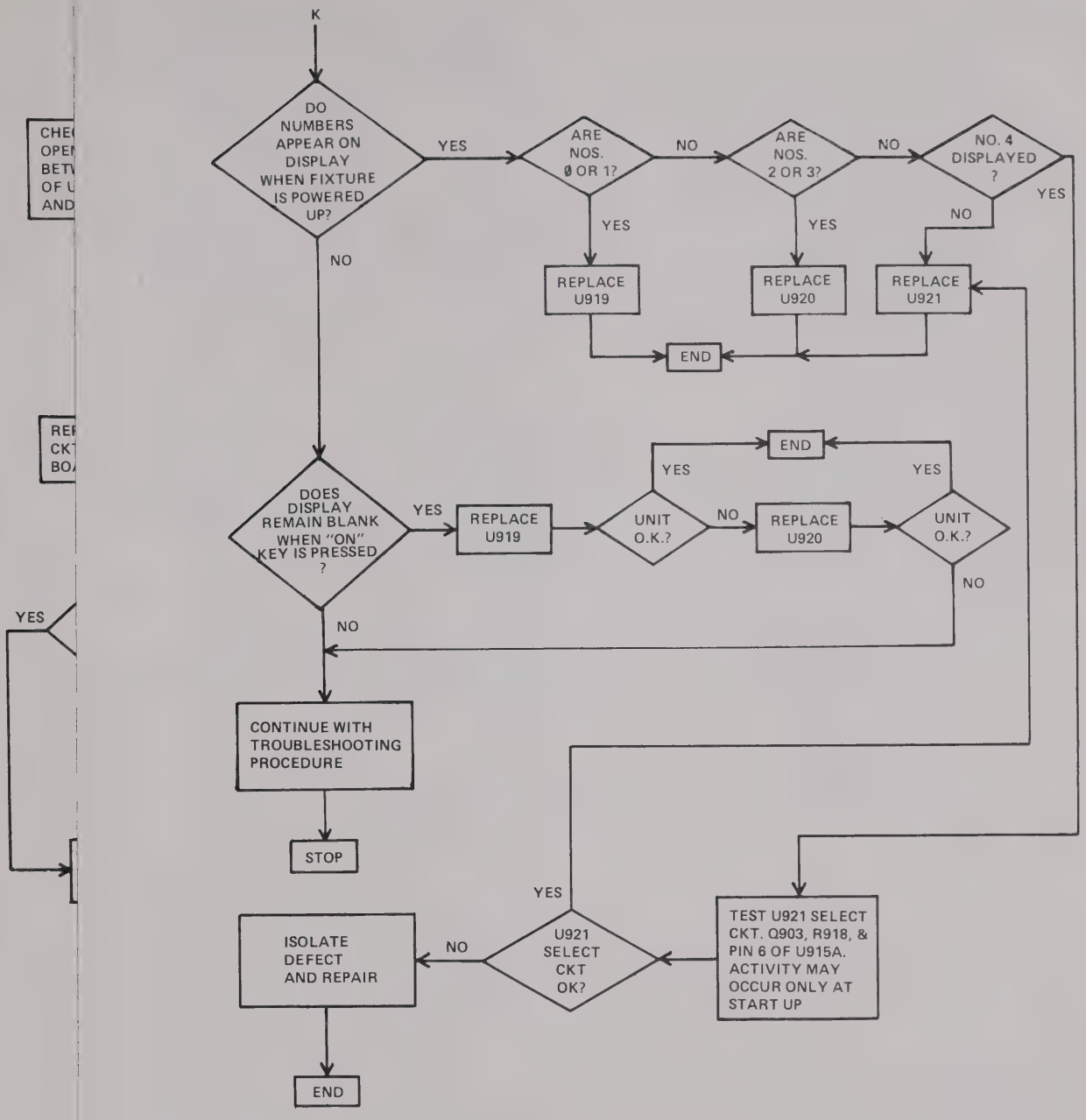
(2) Light Pen Interface Board Troubleshooting Procedure

The following procedures and corresponding suggested remedies are keyed to the detailed Interface Board Troubleshooting Flow Charts, Figures 35, 36, and 37.

Before starting these troubleshooting procedures, complete the ones listed in preceding paragraph 8.b. In any case, the Preliminary Test Setup, outlined in paragraph 8.b., must be done. Upon completion of the last procedure in paragraph 8.b., continue troubleshooting using the following:

(a) Supplementary Test Setup For Light Pen Circuitry Testing

- Place the "EXTERNAL WAND/LP DIAGNOSTIC" switch in the "LP DIAGNOSTIC" position.
- Actuate "PWR RES" button on fixture and observe "RAM TEST 60" on display.
- Actuate the L key to enter the home position of the light pen tests. Observe the "LP TEST NO" on display.
- Verify that the +5.5 V fixture supply is within ±0.03 V. Adjust if necessary.



DEPF-9195-A

Figure 31. Processor Board Troubleshooting Flow Chart (Part 1)

PROCEDURE (Symptom)	REMEDY (Figures 31 and 32)
Press Ø key (or close S12 on fixture). Keys transmitter and modulates via Q line.	Entry point T
Press S key (or close S5 on fixture). Display is blanked and a low frequency tone is heard from speaker.	Entry point T
Press SPACE key (or close S6 on fixture). Display shows flag line inputs. Lower supply voltage until flag line 4 shows character L (trip voltage is 6.0 to 6.5 V).	Entry point U

NOTE

Complete the following procedures only if the processor board under test contains optional light pen circuitry.

PROCEDURE (Symptom)	REMEDY (Figure 32)
Reset power (enter 60-second RAM test) actuate the L key to enter the Light Pen home position. Observe the "LP TEST NO" on display. Using an oscilloscope, probe pins 4 and 7 of U902. Observe 3 μs pulses at an approximate repetition rate of 600 μs.	Entry point V
Pulses should be >5 V in amplitude.	Entry point W
Using an oscilloscope, probe cathodes of CR902 and CR903 and observe stretched pulses. The pulses should be between 80 μs and 160 μs wide at the +3 Vdc level.	Entry point X
Observe "LP PWR" lamp switching on and off with each push of the P key. Observe "2/3 RATIO" lamp switching on and off with each push of the R key.	Entry point Y
From home position, push the "5" key to enter the sample/hold leakage test. Observe the "POS S/H L ?" display. Verify that the "S/H" lamp is on. Push the L key, "S/H" lamp should go off and the prompt will reappear in ≃10 seconds after alert is sounded. Push key "H" to return to home position.	Entry point Z

d. Light Pen Circuits Troubleshooting Procedures

Before troubleshooting the light pen circuits, you must complete the preliminary processor and interface board tests outlined in preceding paragraphs 8.b. and 8.c. The following tests relate only to the NKN6259A light pen connector board and the NLN7218A interface board with light pen circuitry. Tests concerning the NLN7219A processor board with light pen circuits are contained in paragraph c.

(1) General Overall Troubleshooting Chart

PROCEDURE (Symptom)	REMEDY (Figure 33)
Unit does not detect white (display does not blank when light pen is placed on white surface).	Entry point A
Light pen detects white but does not enter data (with beep alert tone) when code is scanned.	Entry point B
Unit always gives error indication (one beep alert tone followed by three beep alert tones).	Entry point C

(2) Light Pen Interface Board Troubleshooting Procedure

The following procedures and corresponding suggested remedies are keyed to the detailed Interface Board Troubleshooting Flow Charts, Figures 35, 36, and 37.

Before starting these troubleshooting procedures, complete the ones listed in preceding paragraph 8.b. In any case, the Preliminary Test Setup, outlined in paragraph 8.b., must be done. Upon completion of the last procedure in paragraph 8.b., continue troubleshooting using the following:

(a) Supplementary Test Setup For Light Pen Circuitry Testing

- Place the "EXTERNAL WAND/LP DIAGNOSTIC" switch in the "LP DIAGNOSTIC" position.
- Actuate "PWR RES" button on fixture and observe "RAM TEST 60" on display.
- Actuate the L key to enter the home position of the light pen tests. Observe the "LP TEST NO" on display.
- Verify that the +5.5 V fixture supply is within ±0.03 V. Adjust if necessary.

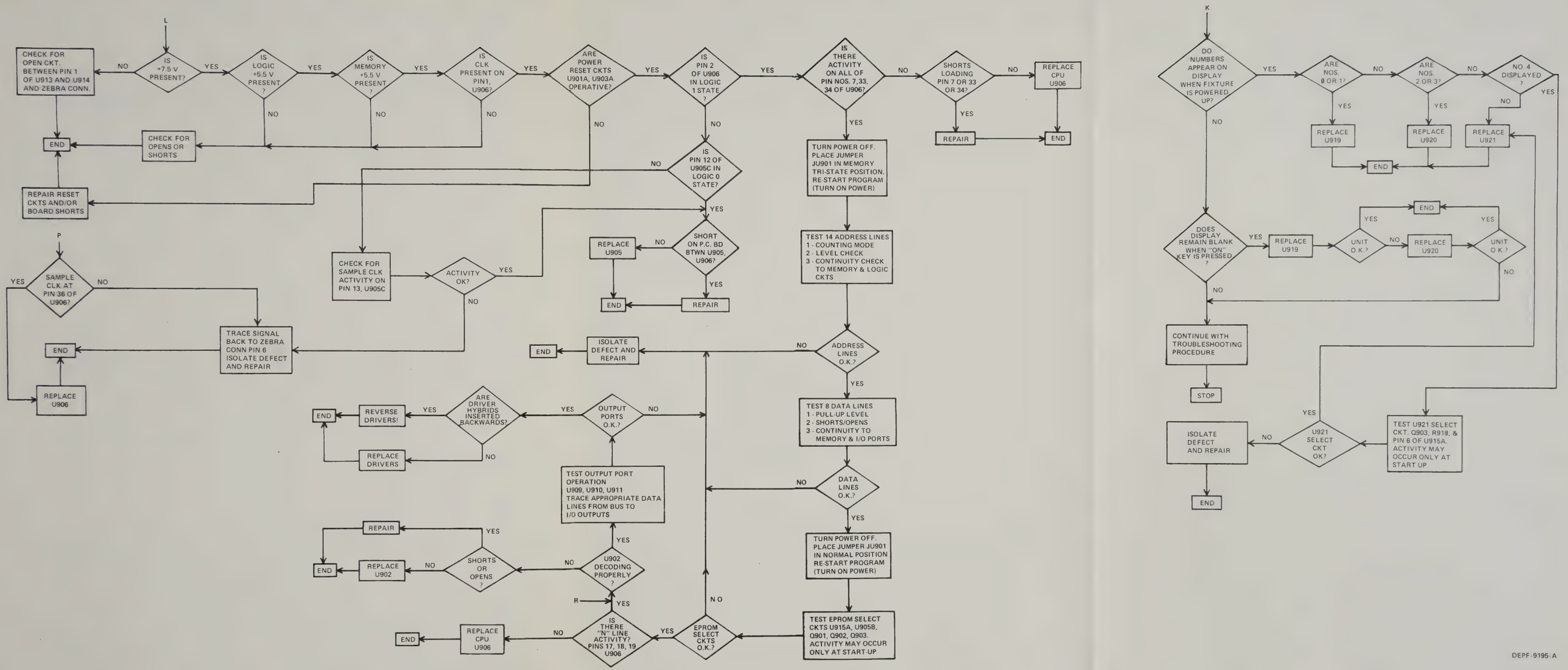

L
CHECK FOR OPEN CKT. BETWEEN PIN 1 OF U913 AND U914 AND ZEBRA CONN.
IS +7.5 V PRESENT?
IS LOGIC +5.5 V PRESENT ?
IS MEMORY +5.5 V PRESENT ?
IS CLK PRESENT ON PIN1, U906?
ARE POWER RESET CKTS U901A, U903A OPERATIVE?
IS PIN 2 OF U906 IN LOGIC 1 STATE ?
IS THERE ACTIVITY ON ALL OF PIN NOS. 7,33, 34 OF U906?
SHORTS LOADING PIN 7 OR 33 OR 34?
REPLACE CPU U906
REPAIR
END
CHECK FOR OPENS OR SHORTS
REPAIR RESET CKTS AND/OR BOARD SHORTS
IS PIN 12 OF U905C IN LOGIC 0 STATE?
TURN POWER OFF. PLACE JUMPER JU901 IN MEMORY TRI-STATE POSITION. RE-START PROGRAM (TURN ON POWER)
P
SAMPLE CLK AT PIN 36 OF U906?
CHECK FOR SAMPLE CLK ACTIVITY ON PIN 13, U905C
ACTIVITY OK?
SHORT ON P.C. BD BTWN U905, U906?
REPLACE U905
TEST 14 ADDRESS LINES 1 - COUNTING MODE 2 - LEVEL CHECK 3 - CONTINUITY CHECK TO MEMORY & LOGIC CKTS
TRACE SIGNAL BACK TO ZEBRA CONN PIN 6 ISOLATE DEFECT AND REPAIR
REPLACE U906
ISOLATE DEFECT AND REPAIR
ADDRESS LINES O.K.?
TEST 8 DATA LINES 1 - PULL-UP LEVEL 2 - SHORTS/OPENS 3 - CONTINUITY TO MEMORY & I/O PORTS
REVERSE DRIVERS!
ARE DRIVER HYBRIDS INSERTED BACKWARDS?
OUTPUT PORTS O.K.?
REPLACE DRIVERS
TEST OUTPUT PORT OPERATION U909, U910, U911 TRACE APPROPRIATE DATA LINES FROM BUS TO I/O OUTPUTS
DATA LINES O.K.?
TURN POWER OFF. PLACE JUMPER JU901 IN NORMAL POSITION RE-START PROGRAM (TURN ON POWER)
REPAIR
REPLACE U902
SHORTS OR OPENS ?
U902 DECODING PROPERLY ?
R
IS THERE "N" LINE ACTIVITY? PINS 17, 18, 19 U906
REPLACE CPU U906
EPROM SELECT CKTS O.K.?
TEST EPROM SELECT CKTS U915A, U905B, Q901, Q902, Q903. ACTIVITY MAY OCCUR ONLY AT START-UP
K
DO NUMBERS APPEAR ON DISPLAY WHEN FIXTURE IS POWERED UP?
ARE NOS. 0 OR 1?
ARE NOS. 2 OR 3?
NO. 4 DISPLAYED ?
REPLACE U919
REPLACE U920
REPLACE U921
DOES DISPLAY REMAIN BLANK WHEN "ON" KEY IS PRESSED ?
UNIT O.K.?
CONTINUE WITH TROUBLESHOOTING PROCEDURE
STOP
ISOLATE DEFECT AND REPAIR
U921 SELECT CKT OK?
TEST U921 SELECT CKT. Q903, R918, & PIN 6 OF U915A. ACTIVITY MAY OCCUR ONLY AT START UP
DEPF-9195-A

Figure 31. Processor Board Troubleshooting Flow Chart (Part 1)

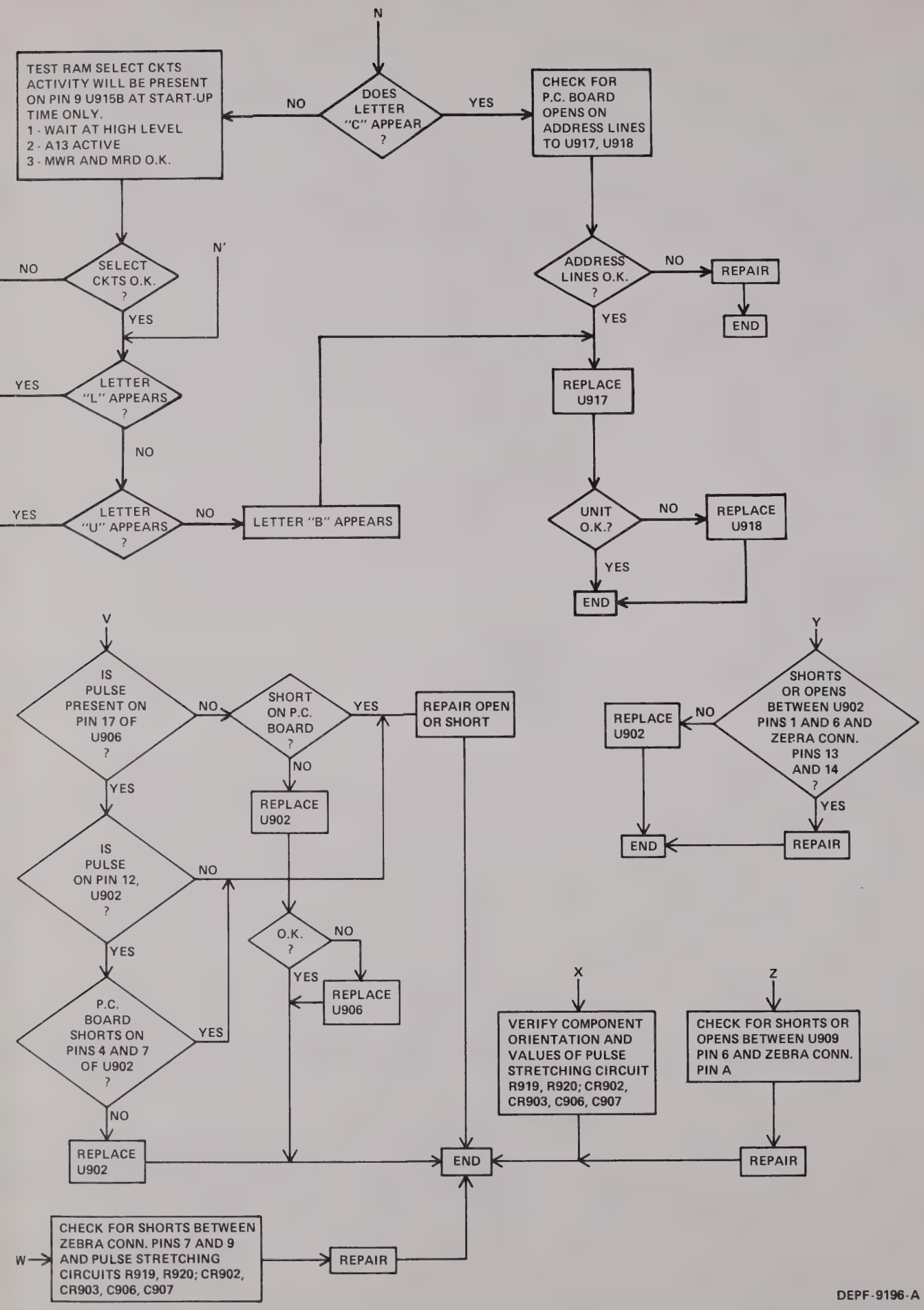


 Figure 32. Processor Board Troubleshooting Flow Chart (Part 2)

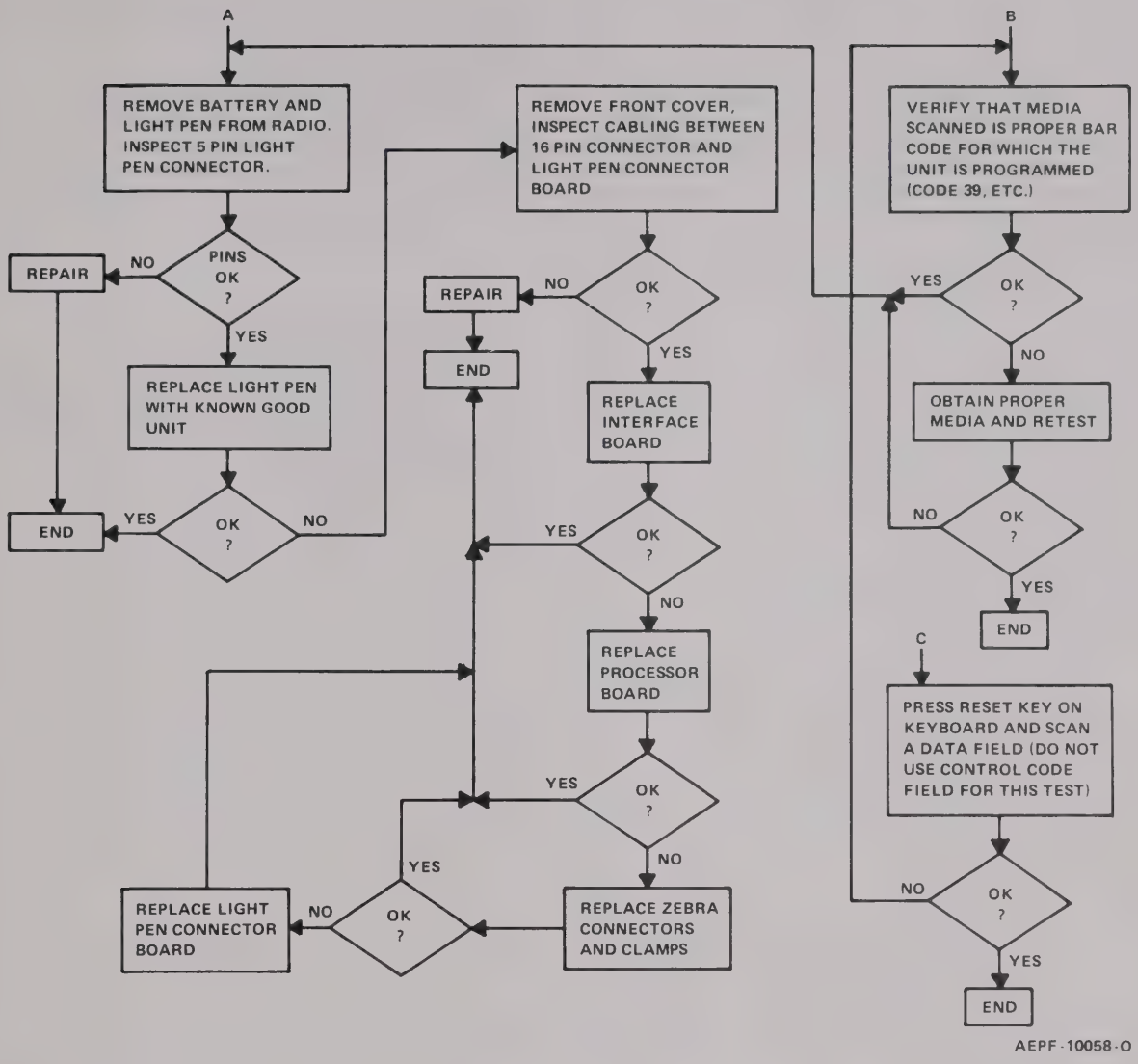


Figure 33. General Troubleshooting Flow Chart, Light Pen

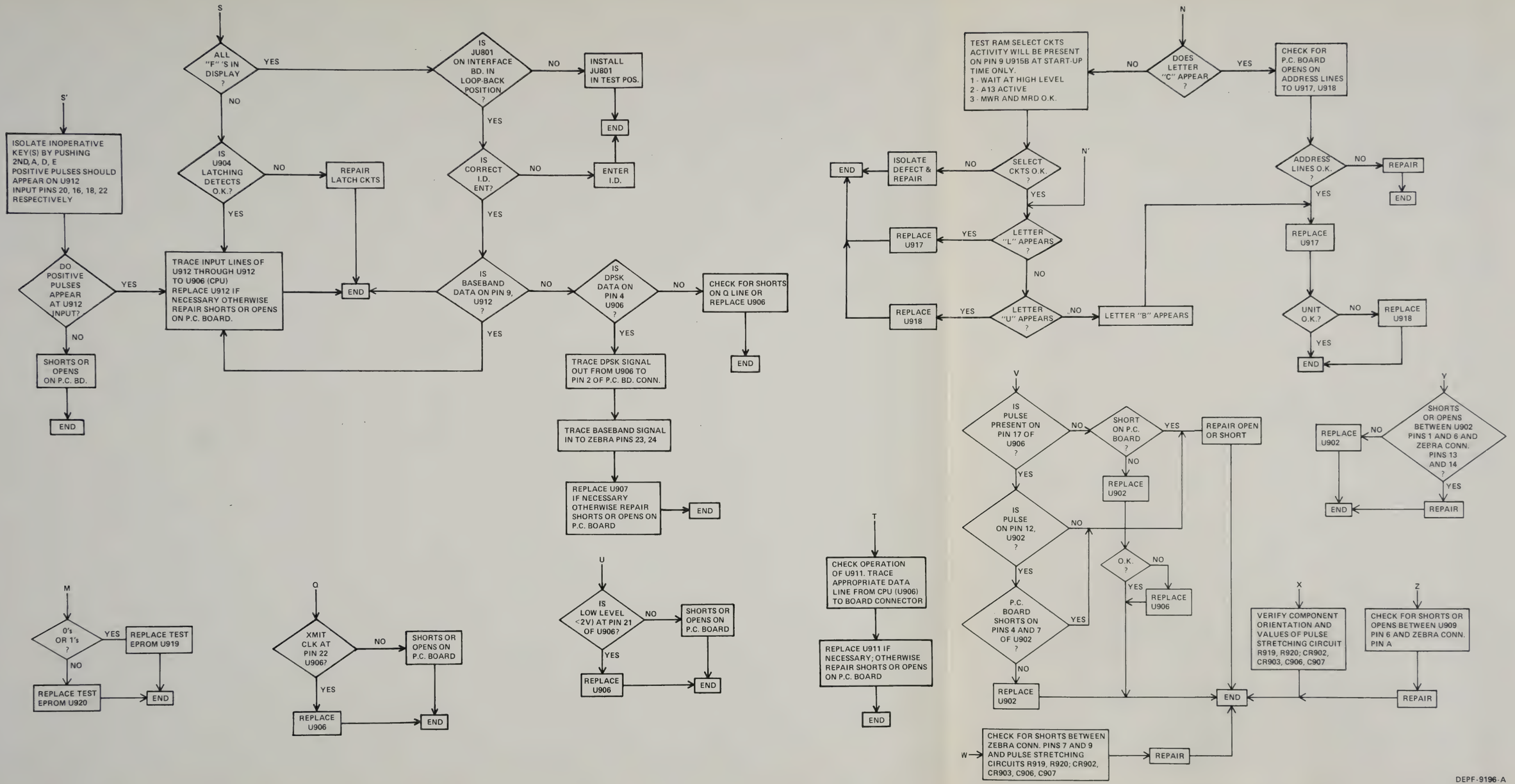
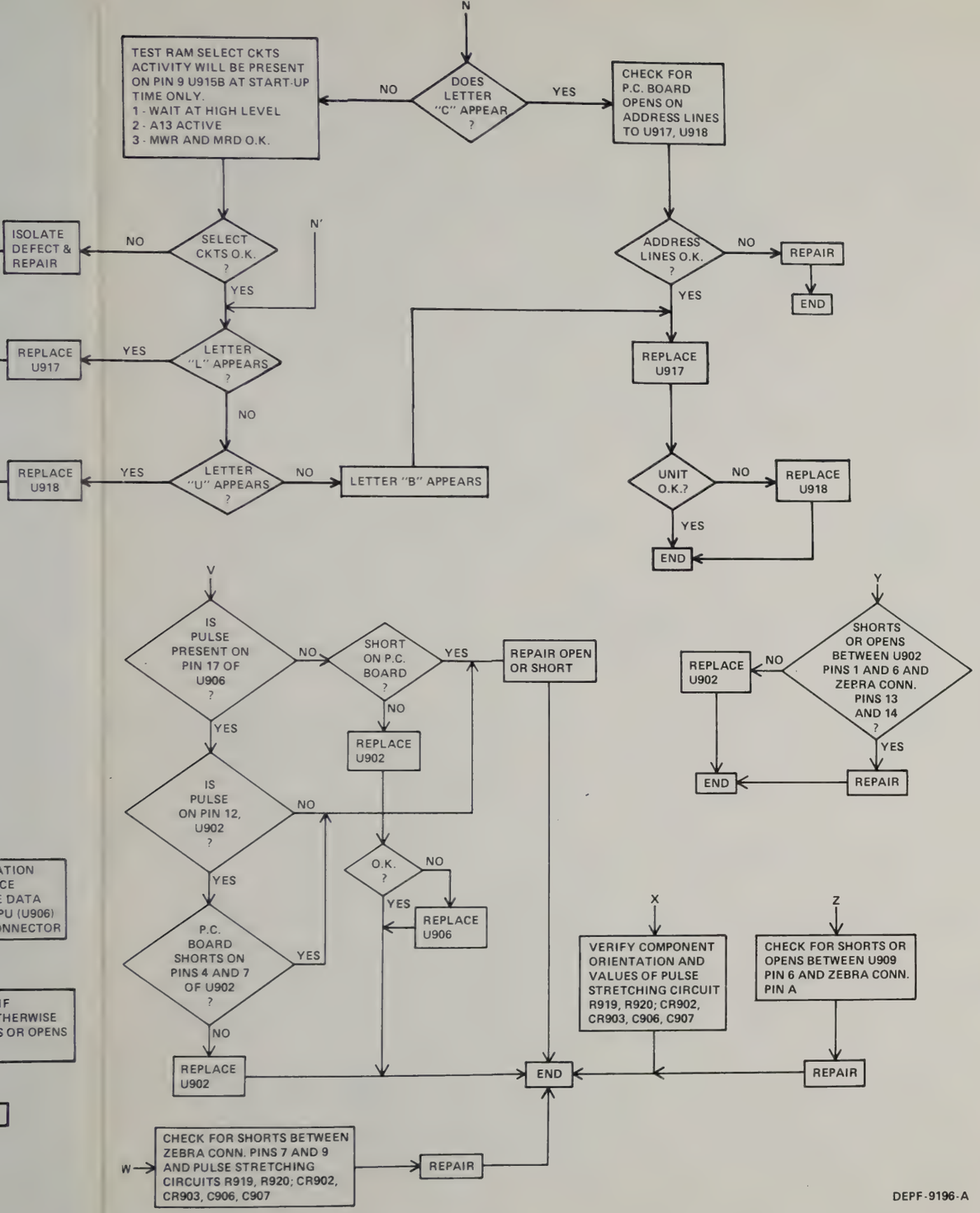


Figure 32. Processor Board Troubleshooting Flow Chart (Part 2)



52 *Figure 32. Processor Board Troubleshooting Flow Chart (Part 2)*

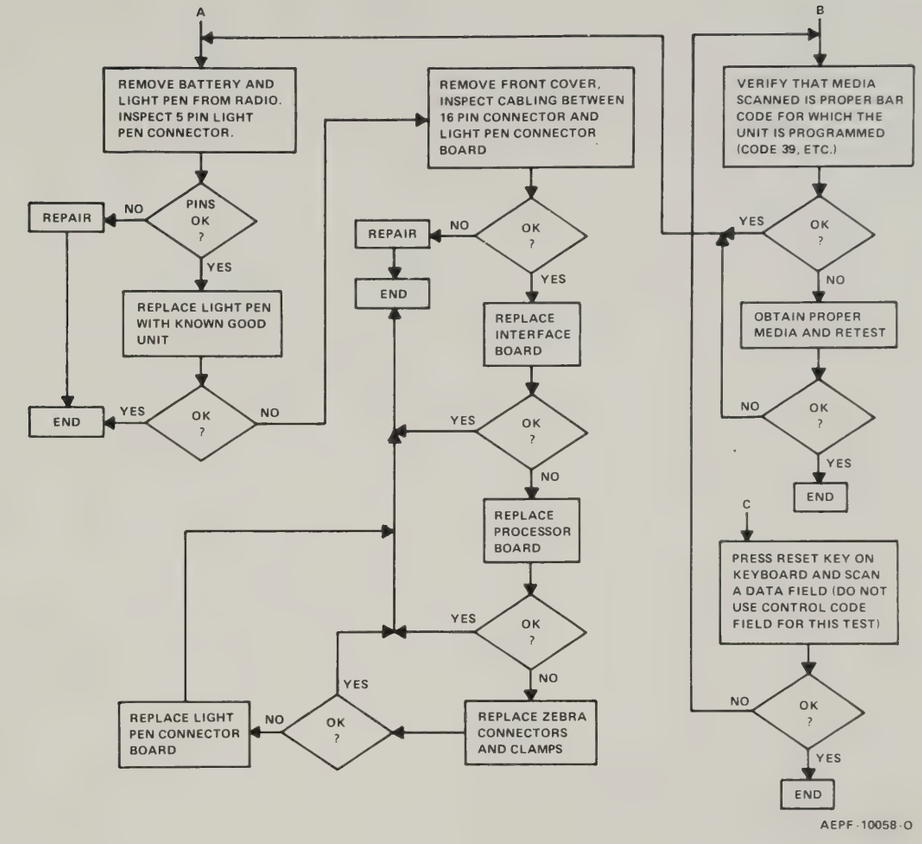


Figure 33. General Troubleshooting Flow Chart, Light Pen

(b) Troubleshooting Procedures

Follow these test procedures until a failure mode is encountered; then refer to the designated flow chart entry point.

PROCEDURE (Symptom)	REMEDY (Figure 35)
After setup, verify that U816 pin 1 voltage is at high level (> +5.25 V) and "LED PWR" lamp is ON. Actuate the "P" key, voltage should go to a low level (< +0.3 V) and lamp should switch off. Subsequent pushes of the "P" key should toggle the voltage in synchronism with the "LED PWR" lamp.	Entry point A
Measure voltage at U816 pin 13, which should be at a high level (> +5.25 V) and the "2/3 RATIO" fixture lamp should be on. Actuate the "R" key, voltage should switch to the low level (< +0.3 V) and the lamp should be off. Subsequent pushes of the "R" key should toggle the voltage in synchronism with the "2/3 RATIO" lamp.	Entry point B
Measure the "4.2 V LP" voltage with the "LED PWR" lamp on. (Actuate the "P" key if lamp is off.) Voltage should be +4.2 V ±0.2 V. Turn lamp off by pushing the "P" key. Measure voltage which should be 0 V ±0.2 V.	Entry point C

- **Light Pen Test #1 (End to End)**

PROCEDURE (Symptom)	REMEDY (Figure 35)
Set rotary switch to position 1. Actuate the "1" key to enter "LP TEST #1." Observe "END TO END PASS" on display. If display shows "END TO END FAIL," troubleshoot, otherwise push key "H" to return to home position to continue tests.	Entry point D

- **Light Pen Test #2 (First Stage Gain)**

PROCEDURE (Symptom)	REMEDY (Figure 36)
Set rotary switch to position 3. Actuate the "2" key to enter "LP TEST #2." Verify the display prompt, "1st STAGE GAIN." Actuate the "1" key. Verify that the "Q" lamp is on. Verify that the voltage at U807 pin 8 is between +3.46 V and +3.90 V. Actuate the "Ø" key. Verify that the "Q" lamp is off. Verify that the voltage at U807 pin 8 is between +0.92 V and +1.23 V. Set rotary switch to position 2. Verify that the voltage at U807 pin 8 is between +5.50 V and +6.00 V. Push key "H" to return to home position to continue tests.	Entry point E

- **Light Pen Test #3 (Ratio Test)**

PROCEDURE (Symptom)	REMEDY (Figure 36)
Set rotary switch to position 3. Actuate the "3" key to enter "LP TEST #3." Verify the display prompt, "RATIO TEST." Verify that the voltage at U808 pin 8 is between +1.65 V and +2.17 V and that the "2/3 RATIO" lamp is off. (Actuate the "R" to turn lamp off if necessary.) Turn lamp on via the "R" key. Verify that the voltage at U808 pin 8 is between +2.42 V and +3.16 V. Push key "H" to return to home position to continue tests.	Entry point F

- **Light Pen Test #4 (Positive/Negative Peak Detect Test)**

PROCEDURE (Symptom)	REMEDY (Figures 36 and 37)
Set rotary switch to position 3, then actuate the "4" key to start the "LP TEST #4." Verify the display prompt "POS PK DT L ? D ? " Measure the voltage at U814 pin 1. Actuate the "L" key, then verify that the voltage does not decrease by more than 1.0 V before the Alert Tone sounds.	Entry point G
When the display prompt reappears, perform the preceding test again. This time actuate the "D" key instead of the "L" key. When the Alert Tone sounds, the voltage should have decreased by a minimum of 1.5 V.	Entry point H
When the display prompt reappears, actuate the "Ø" key to obtain the display prompt "NEG PK DT L ? D ? " Measure the voltage at U814 pin 7. Actuate the "L" key, then verify that the voltage does not increase by more than 1.0 V before the Alert Tone sounds.	Entry point J
When the display prompt reappears, perform the preceding test again. This time actuate the "D" key instead of the "L" key. When the Alert Tone sounds, the voltage should have increased by a minimum of 1.5 V. Push key "H" to return to home position to continue tests.	Entry point K

- **Light Pen Test #5 (Positive/Negative Sample/Hold Test)**

PROCEDURE (Symptom)	REMEDY (Figure 36)
Set rotary switch to position 3. Actuate the "5" key to start the "LP TEST #5" and obtain the display prompt "POS S/H L ?" Measure the voltage at U808 pin 14. Actuate the "L" key, then verify that the voltage does not decrease by more than 200 mV before the Alert Tone sounds.	Entry point L
When the display prompt reappears, actuate the "Ø" key to obtain the display prompt "NEG S/H L ?" Measure voltage at U808 pin 14. Actuate the "L" key, then verify that the voltage does not increase by more than 200 mV before the Alert Tone sounds. Push key "H" to return to home position to continue tests.	Entry point M

- **Light Pen Test #6 (Hysteresis Positive/Negative)**

PROCEDURE (Symptom)	REMEDY (Figure 37)
Set rotary switch to position 4. Actuate the "6" key to start "LP TEST #6" and obtain the display prompt "HYS HIGH LOW." The display will blank (for ≃1 sec.) then return with "HYS HIGH P LOW." After a second blank time the display should return with "HYS HIGH P LOW P." If either or both the first and second "P" in the display is replaced (either intermittently or constantly) with "F" after subsequent blank and returns, then troubleshoot. (Allow a minimum of 6 cycles of blanks and returns before returning to home position to assure non-marginal conditions.) Push key "H" to return to home position.	Entry point N

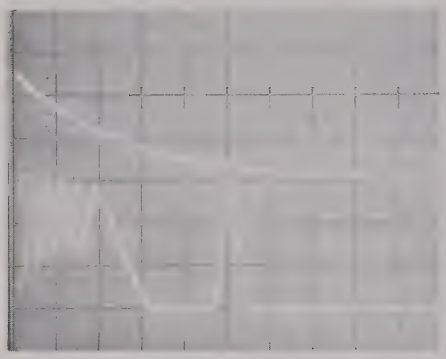


PHOTO 1

PHOTO 1: Top trace is the control line for the positive peak detector discharge switch monitored at pin 5, U815. Bottom trace is the output of the positive peak detector op amp monitored at pin 1, U808.

Oscilloscope Settings:
Horizontal – Time Base = 100 us/Div Alternate Sweep (single shots).
Vertical – (Top Trace) 2 V/Div DC coupled; ground is center line.
– (Bottom Trace) 1 V/Div DC coupled; ground is second line from bottom.

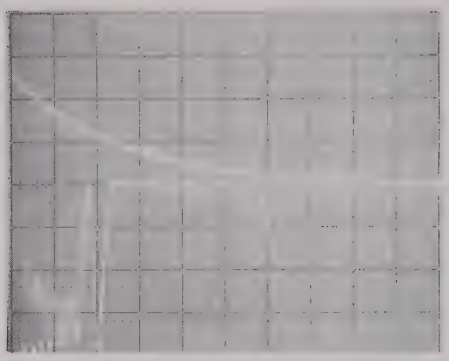


PHOTO 2

PHOTO 2: Top trace is control line for negative peak detector discharge switch monitored at pin 6, U815. Bottom trace is the output of the negative peak detector op amp monitored at pin 7, U808.

Oscilloscope Settings:
Horizontal – Time Base = 100 us/Div Alternate Sweep (single shots).
Vertical – (Top Trace) 2 V/Div DC coupled; ground is center line.
– (Bottom Trace) 1 V/Div DC coupled, center line = +5.5 V.

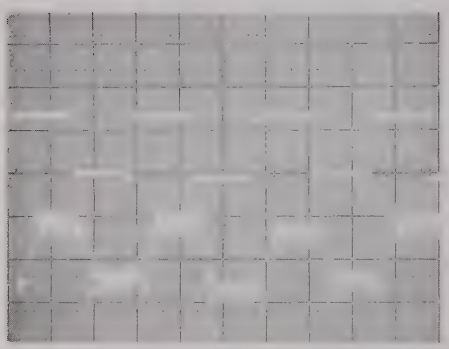


PHOTO 3

PHOTO 3: Top trace monitored at pin 10, U807 (minimum input signal $\simeq$ 70 mV). Bottom trace is the threshold input to the light pen output op amp monitored at pin 13, U807.

Oscilloscope Settings:
Horizontal – Time Base = 500 us/Div, Chopped Sweep.
Vertical – (Top Trace) 50 mV/Div AC coupled.
– (Bottom Trace) 50 mV/Div AC coupled.

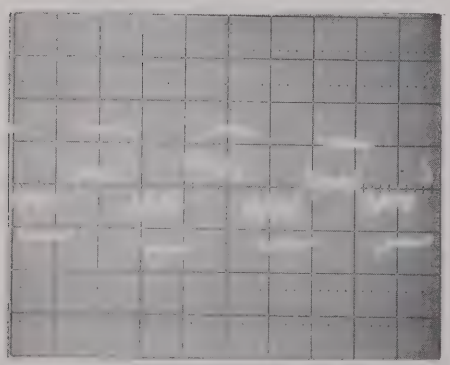


PHOTO 4

PHOTO 4: Trace with larger amplitude monitored at junction of hysteresis diodes (CR805 and CR806) and R822 and R821. Trace with noise and smaller amplitude monitored at pin 8, U808, which is the buffered threshold input.

Oscilloscope Settings:
Horizontal – Time Base = 500 us/Div, Chopped Sweep.
Vertical – 100 mV/Div, AC coupled.

NOTE: These waveforms were displayed on a HP1741A storage oscilloscope with a HP197B camera. The grid was exposed with a minimum persistance at 1/4 f 8 (+). The waveforms were exposed with a maximum persistance at 1/2 f 8 (+). These photos are referenced in Flow Chart D, Figure 35.

 Figure 34. Light Pen Circuit Photos

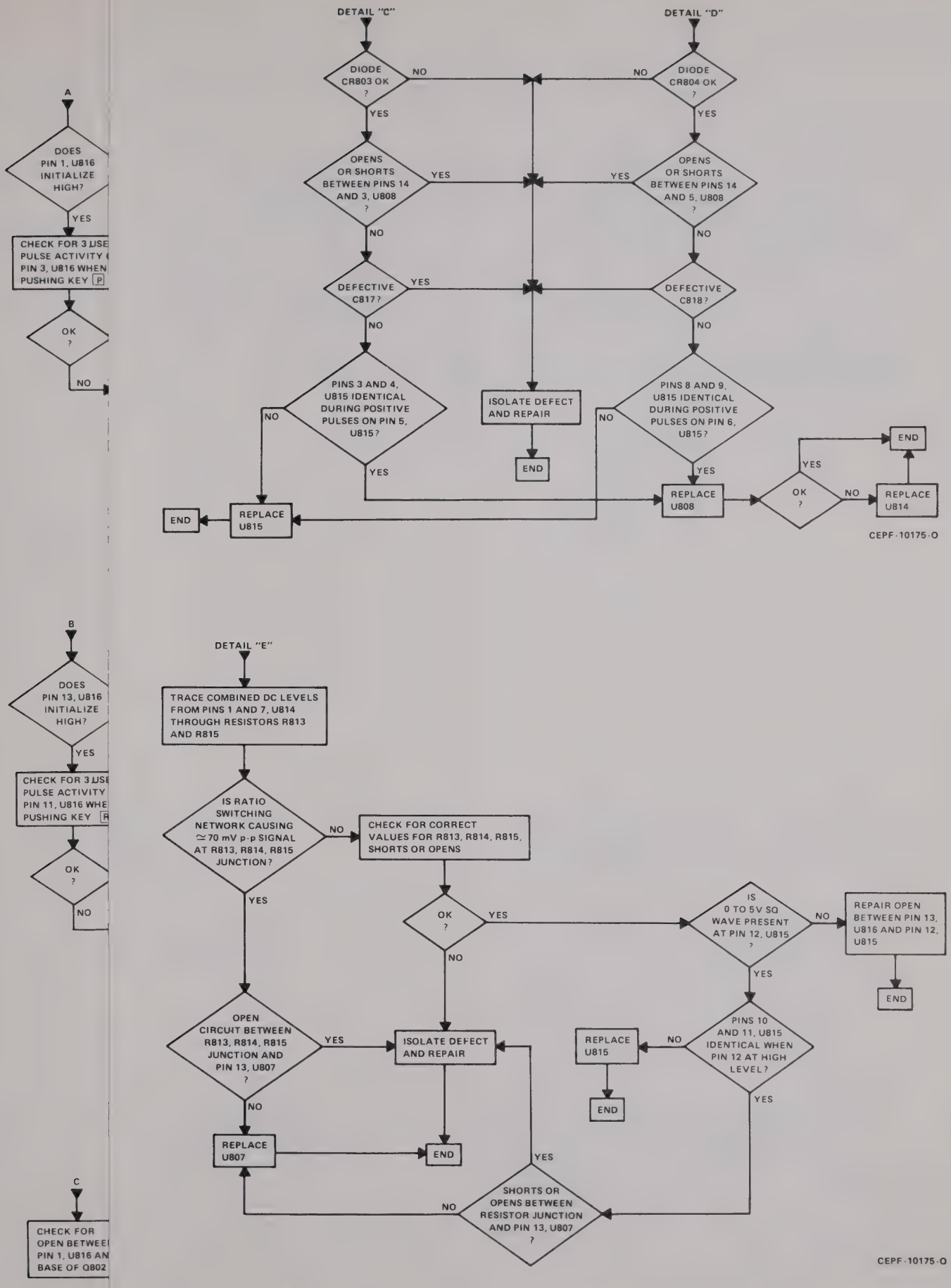


Figure 35. Light Pen Interface Board Troubleshooting Flow Chart (Part 1)

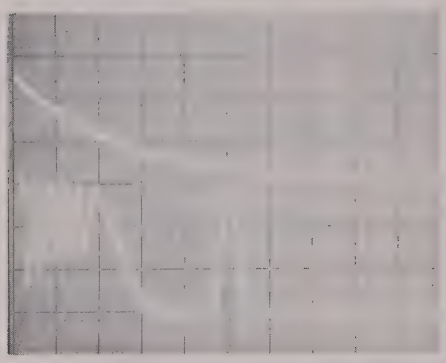


PHOTO 1

PHOTO 1: Top trace is the control line for the positive peak detector discharge switch monitored at pin 5, U815. Bottom trace is the output of the positive peak detector op amp monitored at pin 1, U808.

Oscilloscope Settings:
Horizontal – Time Base = 100 us/Div Alternate Sweep (single shots).
Vertical – (Top Trace) 2 V/Div DC coupled; ground is center line.
– (Bottom Trace) 1 V/Div DC coupled; ground is second line from bottom.

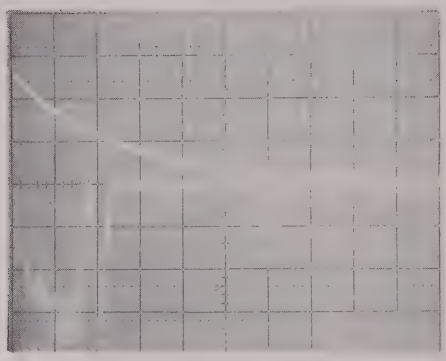


PHOTO 2

PHOTO 2: Top trace is control line for negative peak detector discharge switch monitored at pin 6, U815. Bottom trace is the output of the negative peak detector op amp monitored at pin 7, U808.

Oscilloscope Settings:
Horizontal – Time Base = 100 us/Div Alternate Sweep (single shots).
Vertical – (Top Trace) 2 V/Div DC coupled; ground is center line.
– (Bottom Trace) 1 V/Div DC coupled, center line = +5.5 V.

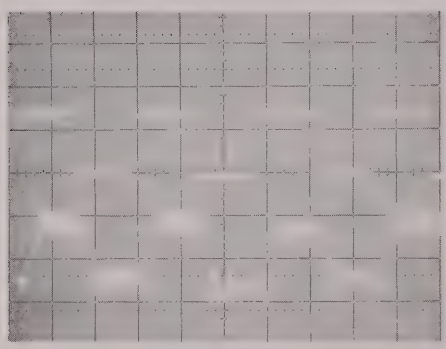


PHOTO 3

PHOTO 3: Top trace monitored at pin 10, U807 (minimum input signal $\simeq$ 70 mV). Bottom trace is the threshold input to the light pen output op amp monitored at pin 13, U807.

Oscilloscope Settings:
Horizontal – Time Base = 500 us/Div, Chopped Sweep.
Vertical – (Top Trace) 50 mV/Div AC coupled.
– (Bottom Trace) 50 mV/Div AC coupled.

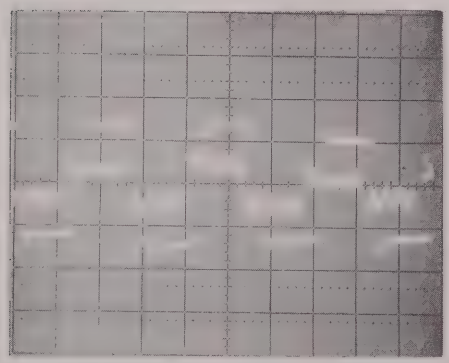


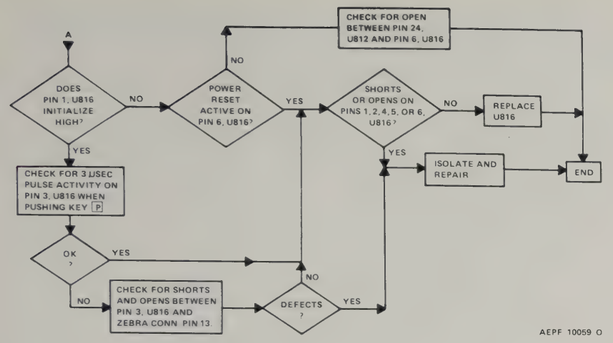
PHOTO 4

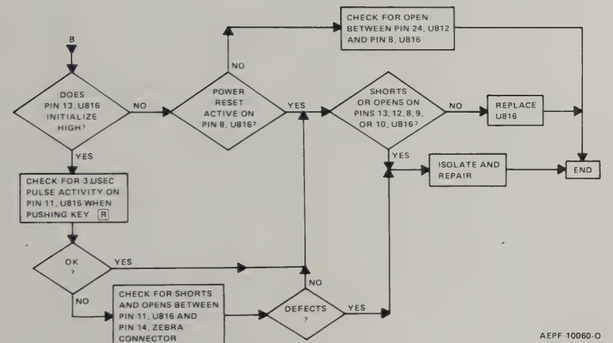
PHOTO 4: Trace with larger amplitude monitored at junction of hysteresis diodes (CR805 and CR806) and R822 and R821. Trace with noise and smaller amplitude monitored at pin 8, U808, which is the buffered threshold input.

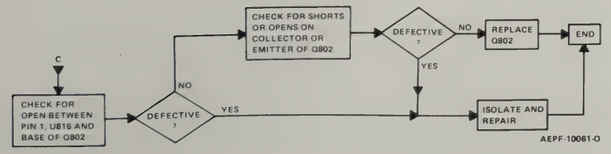
Oscilloscope Settings:
Horizontal – Time Base = 500 us/Div, Chopped Sweep.
Vertical – 100 mV/Div, AC coupled.

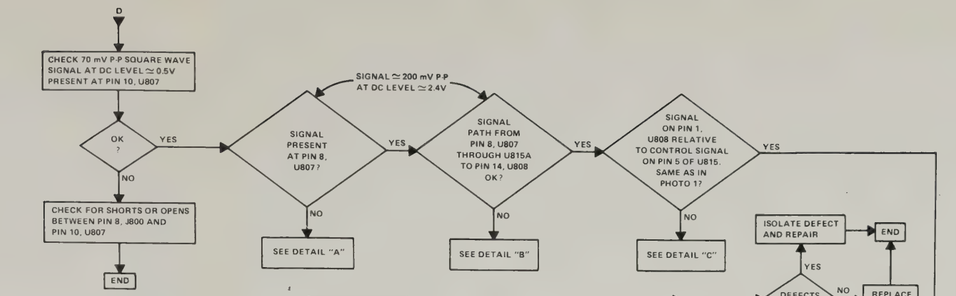
NOTE: These waveforms were displayed on a HP1741A storage oscilloscope with a HP197B camera. The grid was exposed with a minimum persistance at 1/4 f 8 (+). The waveforms were exposed with a maximum persistance at 1/2 f 8 (+). These photos are referenced in Flow Chart D, Figure 35.

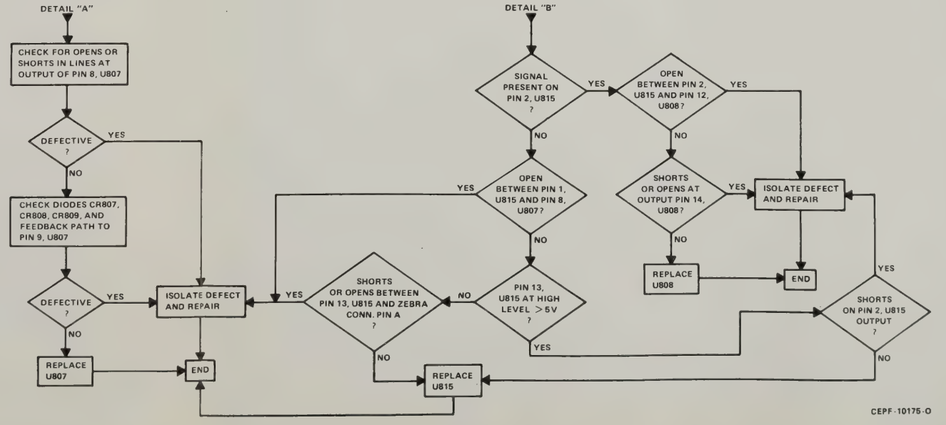
 Figure 34. Light Pen Circuit Photos

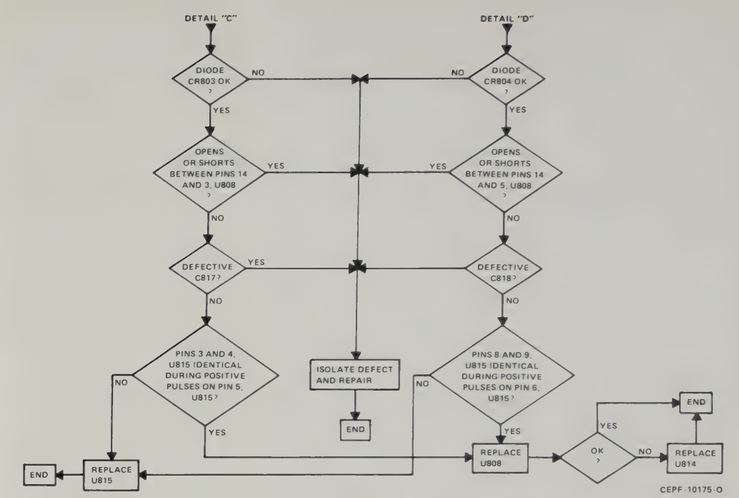







D
CHECK 70 mV P-P SQUARE WAVE SIGNAL AT DC LEVEL ≃ 0.5V PRESENT AT PIN 10, U807
OK ?
YES
NO
CHECK FOR SHORTS OR OPENS BETWEEN PIN 8, J800 AND PIN 10, U807
END
SIGNAL ≃ 200 mV P-P AT DC LEVEL ≃ 2.4V
SIGNAL PRESENT AT PIN 8, U807?
YES
NO
SEE DETAIL "A"
SIGNAL PATH FROM PIN 8, U807 THROUGH U815A TO PIN 14, U808 OK?
YES
NO
SEE DETAIL "B"
SIGNAL ON PIN 1, U808 RELATIVE TO CONTROL SIGNAL ON PIN 5 OF U815, SAME AS IN PHOTO 1?
YES
NO
SEE DETAIL "C"
ISOLATE DEFECT AND REPAIR
END
DEFECTS ?
YES
NO
REPLACE U814
SEE DETAIL "E"
CHECK FOR OPENS AND SHORTS ON PINS 6 OR 7, U814
SEE DETAIL "D"
CHECK FOR OPENS AND SHORTS ON PINS 1 AND 2 OF U814
WAVEFORM AT PIN 13, U807 RELATIVE TO 70 mV INPUT SIGNAL AT PIN 10, U807. SAME AS IN PHOTO 3?
YES
NO
DOES DC LEVEL AT PIN 7, U814 MEASURE ≃ 0.20V LESS THAN PIN 1, U814?
YES
NO
SIGNAL ON PIN 7, U808 RELATIVE TO CONTROL SIGNAL ON PIN 6, U815 SAME AS IN PHOTO 2?
YES
NO
DOES DC LEVEL AT PIN 1, U814 MEASURE ≃ +2.4V?
YES
NO
DEFECTS, SHORTS OR OPENS ?
NO
YES
END
ISOLATE DEFECT AND REPAIR
REPLACE U807
END
CHECK CONTINUITY THROUGH RESISTOR R820 AND CHECK FOR CORRECT VALUES FOR R820, R821
CHECK FOR SHORTS BETWEEN PIN 14, U807 AND R804. CHECK IF POOR ZEBRA CONNECTOR IS AFFECTING DUTY CYCLE OR AMPLITUDE.
DEFECTS ?
YES
NO
ISOLATE DEFECT AND REPAIR
WAVEFORM AT PIN 12, U807 SIMILAR TO WAVEFORM AT PIN 14, U808?
YES
NO
WAVEFORM AT PIN 8, U808 RELATIVE TO WAVEFORM AT JUNCTION OF CR805, CR806, AND R821, R822. SAME AS IN PHOTO 4?
YES
NO
WAVEFORM AT PIN 14, U807 SWINGS BETWEEN ≃0.7V AND ≃ 5.7 V. DUTY CYCLE = 50 ±5%?
YES
NO
SIGNAL PATH OK BETWEEN PIN 14, U807 AND ZEBRA CONNECTOR PIN 11 ?
YES
NO
CHECK ZEBRA CONNECTORS AND CONTINUITY TO PROCESSOR BOARD
END
BEPF-10062-O





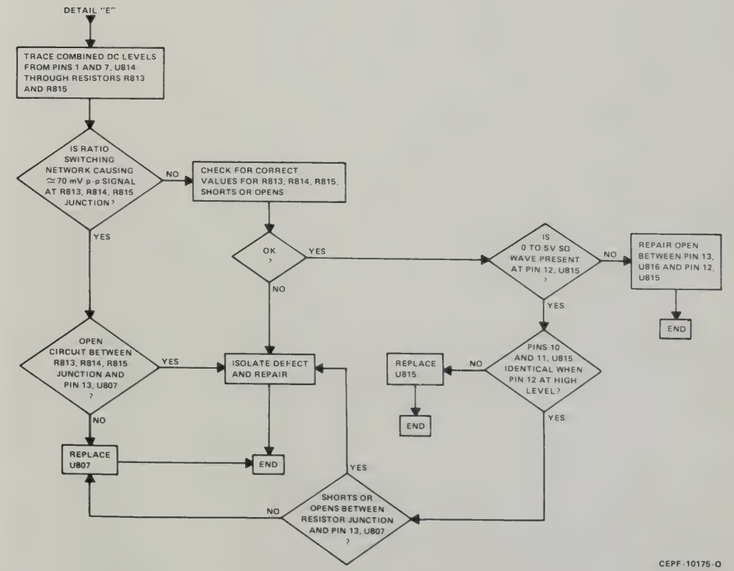
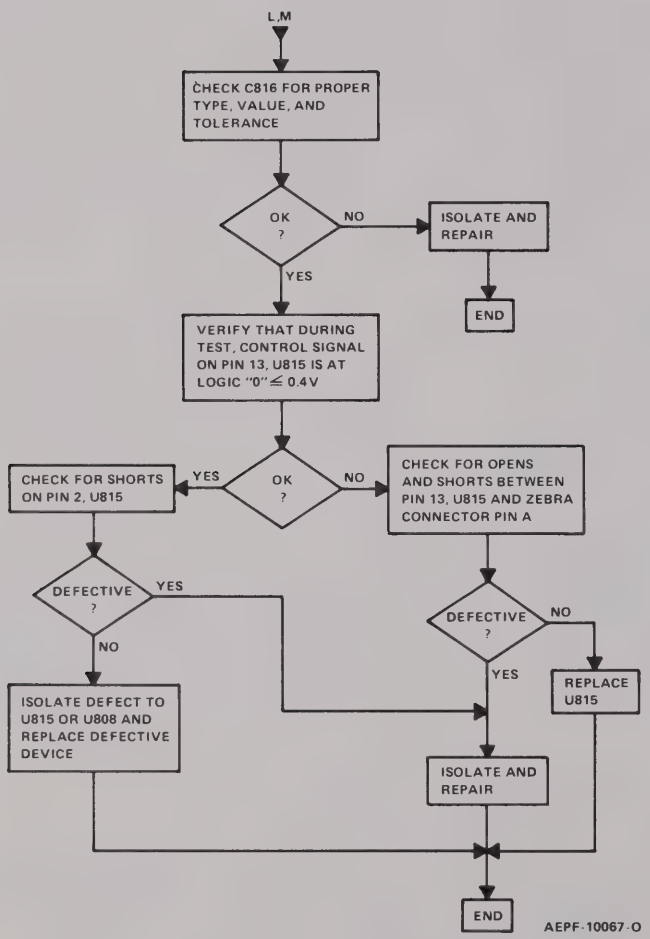

DETAIL "E"
TRACE COMBINED DC LEVELS FROM PINS 1 AND 7, U814 THROUGH RESISTORS R813 AND R815
IS RATIO SWITCHING NETWORK CAUSING ≃70 mV p-p SIGNAL AT R813, R814, R815 JUNCTION ?
YES
NO
CHECK FOR CORRECT VALUES FOR R813, R814, R815, SHORTS OR OPENS
OK ?
YES
NO
IS 0 TO 5V SQ WAVE PRESENT AT PIN 12, U815 ?
NO
YES
REPAIR OPEN BETWEEN PIN 13, U816 AND PIN 12, U815
END
OPEN CIRCUIT BETWEEN R813, R814, R815 JUNCTION AND PIN 13, U807 ?
YES
NO
ISOLATE DEFECT AND REPAIR
REPLACE U815
END
PINS 10 AND 11, U815 IDENTICAL WHEN PIN 12 AT HIGH LEVEL?
YES
NO
REPLACE U807
END
SHORTS OR OPENS BETWEEN RESISTOR JUNCTION AND PIN 13, U807 ?
YES
NO
CEPF-10175-O

Figure 35. Light Pen Interface Board Troubleshooting Flow Chart (Part 1)



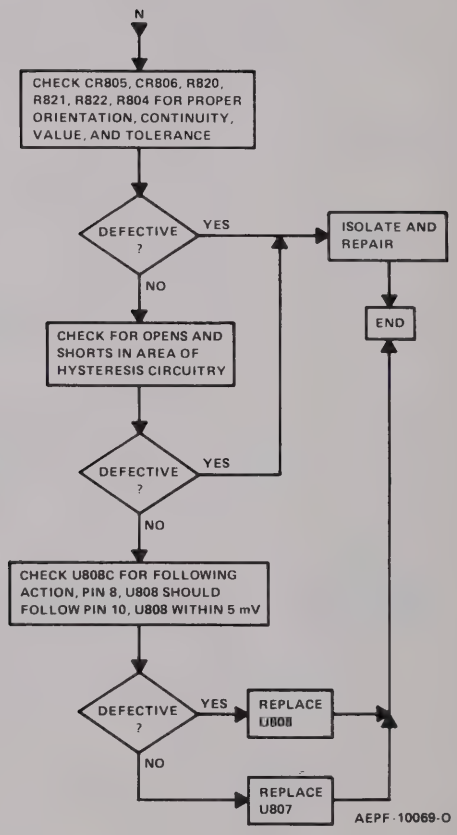


Figure 37. Light Pen Interface Board Troubleshooting Flow Chart (Part 3)

REPAIR, PARTS ORDERING, AND REPLACEMENT

1. MOS CIRCUIT HANDLING PRECAUTIONS

The following handling precautions are recommended for MOS circuits:

NOTE

These precautions are especially important in low humidity conditions.

a. All MOS devices should be stored or transported in conductive material so that all exposed leads are shorted together. MOS devices must not be inserted into conventional plastic "snow" or plastic trays of the type used for storage and transportation of other semiconductor devices.

b. All MOS devices should be placed on a grounded bench surface and the technicians should ground themselves prior to handling devices. This is done most effectively by having the technician wear a conductive wrist strap in series with 100 k ohms to ground. (Motorola ST1191 Wrist Strap is recommended.)

c. Nylon clothing should not be worn while handling MOS circuits.

d. Do not insert or remove MOS devices with power applied. Check all power supplies to be used for testing MOS devices and be certain there are no voltage transients present.

e. When lead straightening, provide ground straps for the apparatus used.

f. When soldering, use a grounded soldering iron.

g. All power should be turned off in a system before printed circuit boards containing MOS devices are inserted or removed.

h. All printed circuit boards containing MOS devices should be provided with shorting straps across the edge connector when being carried or transported.

i. MOS devices should be handled by their packages and not by the leads, if at all possible. Prior to touching the unit, the technician should touch an electrical ground to remove any static charge that may have accumulated. The package and substrate may be electrically common. If so, the reaction of a discharge to the case would cause the same damage as touching the leads.

2. RADIO CIRCUIT BOARD REPAIR

The four-layer radio circuit board presents some new considerations when soldering and unsoldering components. The printed through holes may interconnect two, three, or all four layers of printed circuit. Care should be exercised to avoid pulling the plated circuit out of the hole. If parts under the flex circuit must be replaced, it may be necessary to unsolder part of the flex circuit covering the desired area on the circuit board. Refer to the following paragraph regarding flexible circuits.

When soldering near the module socket pins, use care to avoid accidently getting solder in the guide pin socket, which is open on the end. Insert the module pusher tool into the hole while soldering. Also, be careful not to form solder bridges between module socket pins. Inspect your work for shorts due to solder bridges.

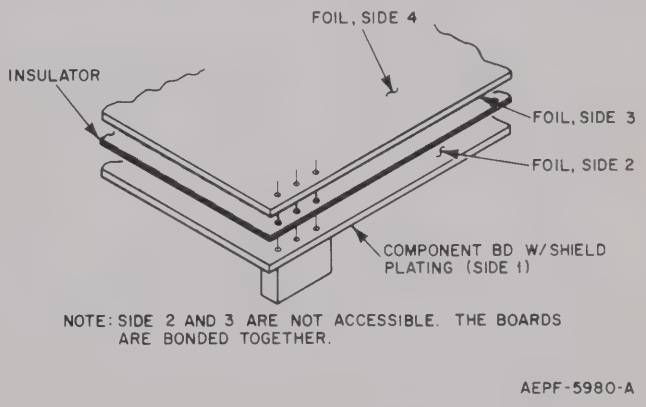

FOIL, SIDE 4
INSULATOR
FOIL, SIDE 3
FOIL, SIDE 2
COMPONENT BD W/SHIELD PLATING (SIDE 1)
NOTE: SIDE 2 AND 3 ARE NOT ACCESSIBLE. THE BOARDS ARE BONDED TOGETHER.
AEPF-5980-A

Figure 38. Typical Four-Layer Board Construction

3. FLEXIBLE CIRCUIT REPAIR

a. General

NOTE

To remove the flex circuit from the radio frame it is not necessary to unsolder socket J302. This socket plugs into the pins on the external accessory connector and can be removed by gently prying it apart.

The flexible circuits are made from a different material than the rigit circuit board and different techniques must be used when soldering.

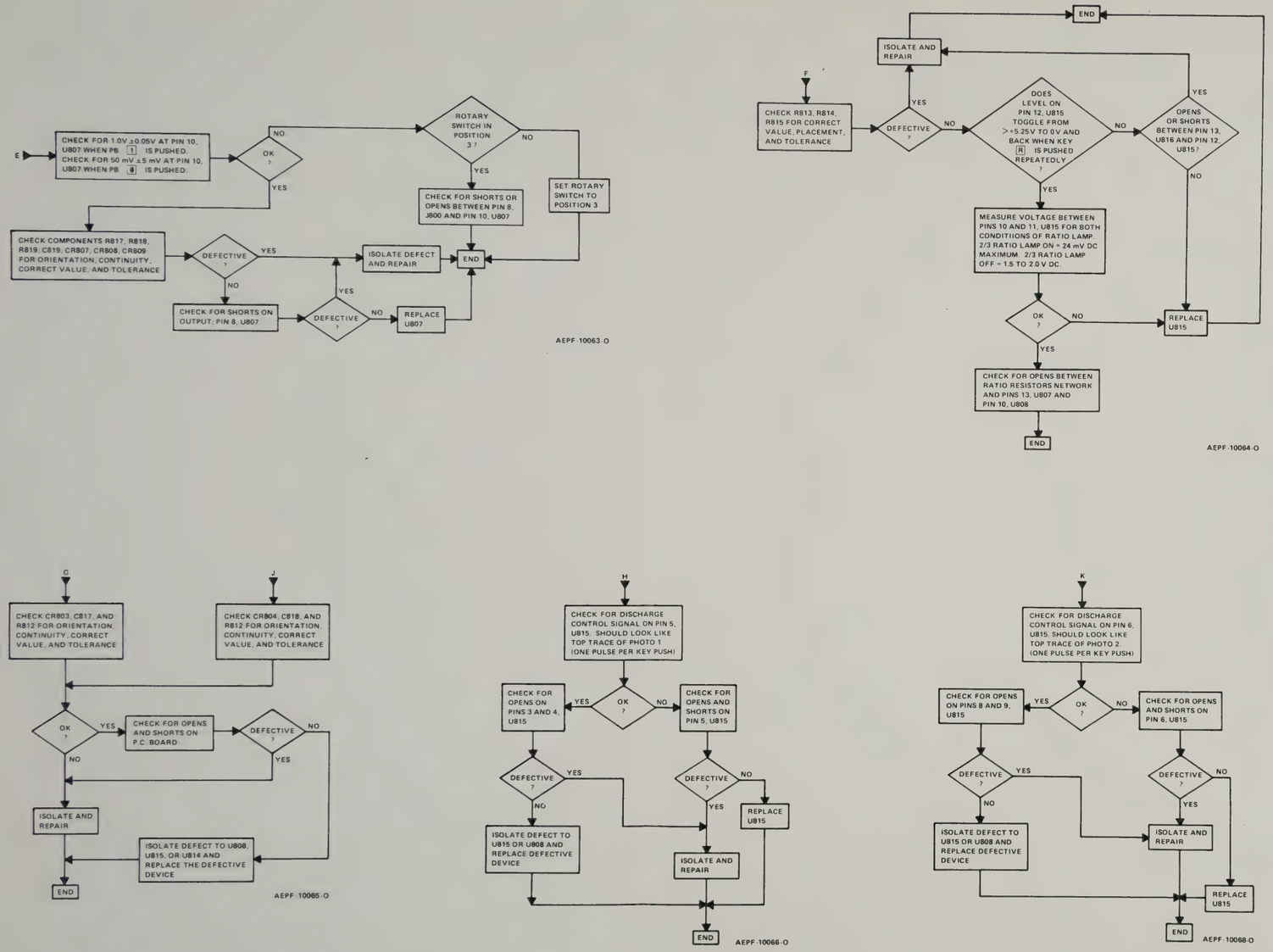

E
CHECK FOR 1.0V ±0.05V AT PIN 10, U807 WHEN PB 1 IS PUSHED. CHECK FOR 50 mV ±5 mV AT PIN 10, U807 WHEN PB 0 IS PUSHED.
OK ?
NO
YES
ROTARY SWITCH IN POSITION 3 ?
NO
YES
SET ROTARY SWITCH TO POSITION 3
CHECK FOR SHORTS OR OPENS BETWEEN PIN 8, J800 AND PIN 10, U807
CHECK COMPONENTS R817, R818, R819, C819, CR807, CR808, CR809 FOR ORIENTATION, CONTINUITY, CORRECT VALUE, AND TOLERANCE
DEFECTIVE ?
YES
NO
ISOLATE DEFECT AND REPAIR
END
CHECK FOR SHORTS ON OUTPUT; PIN 8, U807
DEFECTIVE ?
YES
NO
REPLACE U807
AEPF-10063-O
F
CHECK R813, R814, R815 FOR CORRECT VALUE, PLACEMENT, AND TOLERANCE
DEFECTIVE ?
YES
NO
ISOLATE AND REPAIR
END
DOES LEVEL ON PIN 12, U815 TOGGLE FROM >+5.25 V TO 0 V AND BACK WHEN KEY R IS PUSHED REPEATEDLY ?
NO
YES
OPENS OR SHORTS BETWEEN PIN 13, U816 AND PIN 12, U815?
YES
NO
MEASURE VOLTAGE BETWEEN PINS 10 AND 11, U815 FOR BOTH CONDITIONS OF RATIO LAMP 2/3 RATIO LAMP ON = 24 mV DC MAXIMUM. 2/3 RATIO LAMP OFF = 1.5 TO 2.0 V DC.
OK ?
NO
YES
REPLACE U815
CHECK FOR OPENS BETWEEN RATIO RESISTORS NETWORK AND PINS 13, U807 AND PIN 10, U808
END
AEPF-10064-O
G
CHECK CR803, C817, AND R812 FOR ORIENTATION, CONTINUITY, CORRECT VALUE, AND TOLERANCE
J
CHECK CR804, C818, AND R812 FOR ORIENTATION, CONTINUITY, CORRECT VALUE, AND TOLERANCE
OK ?
YES
NO
CHECK FOR OPENS AND SHORTS ON P.C. BOARD
DEFECTIVE ?
NO
YES
ISOLATE AND REPAIR
ISOLATE DEFECT TO U808, U815, OR U814 AND REPLACE THE DEFECTIVE DEVICE
END
AEPF-10065-O
H
CHECK FOR DISCHARGE CONTROL SIGNAL ON PIN 5, U815. SHOULD LOOK LIKE TOP TRACE OF PHOTO 1 (ONE PULSE PER KEY PUSH)
CHECK FOR OPENS ON PINS 3 AND 4, U815
OK ?
YES
NO
CHECK FOR OPENS AND SHORTS ON PIN 5, U815
DEFECTIVE ?
YES
NO
ISOLATE DEFECT TO U815 OR U808 AND REPLACE DEFECTIVE DEVICE
DEFECTIVE ?
NO
YES
REPLACE U815
ISOLATE AND REPAIR
END
AEPF-10066-O
K
CHECK FOR DISCHARGE CONTROL SIGNAL ON PIN 6, U815. SHOULD LOOK LIKE TOP TRACE OF PHOTO 2. (ONE PULSE PER KEY PUSH)
CHECK FOR OPENS ON PINS 8 AND 9, U815
OK ?
YES
NO
CHECK FOR OPENS AND SHORTS ON PIN 6, U815
DEFECTIVE ?
YES
NO
ISOLATE DEFECT TO U815 OR U808 AND REPLACE DEFECTIVE DEVICE
DEFECTIVE ?
NO
YES
ISOLATE AND REPAIR
REPLACE U815
END
AEPF-10068-O

Figure 36. Light Pen Interface Board Troubleshooting Flow Chart (Part 2)

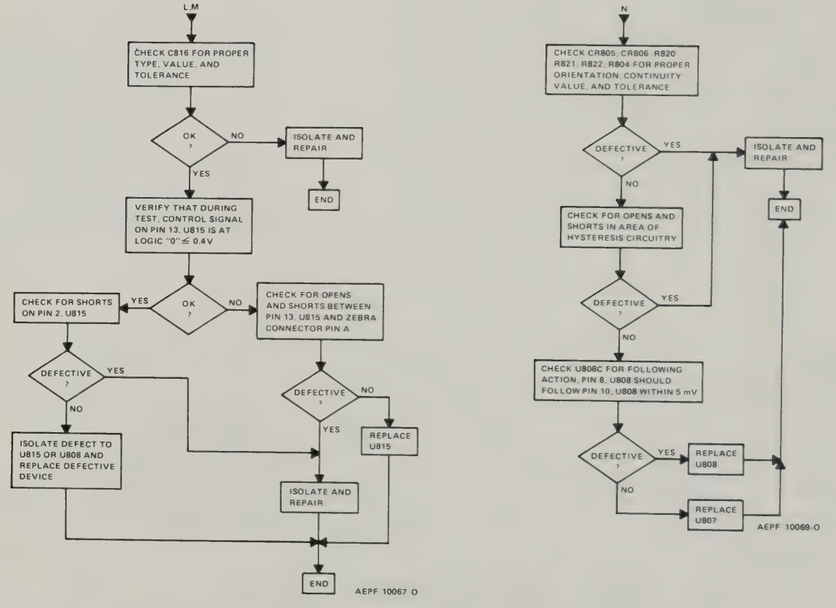


Figure 37. Light Pen Interface Board Troubleshooting Flow Chart (Part 3)

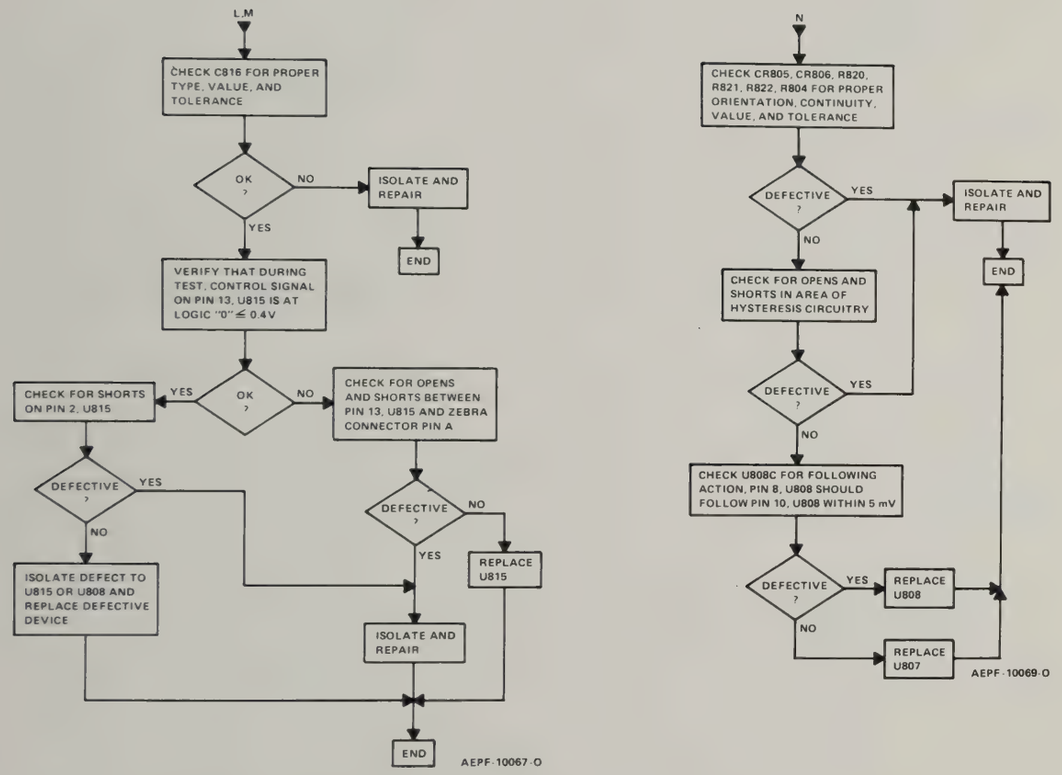


Figure 37. Light Pen Interface Board Troubleshooting Flow Chart (Part 3)

REPAIR, PARTS ORDERING, AND REPLACEMENT

1. MOS CIRCUIT HANDLING PRECAUTIONS

The following handling precautions are recommended for MOS circuits:

NOTE

These precautions are especially important in low humidity conditions.

a. All MOS devices should be stored or transported in conductive material so that all exposed leads are shorted together. MOS devices must not be inserted into conventional plastic "snow" or plastic trays of the type used for storage and transportation of other semiconductor devices.

b. All MOS devices should be placed on a grounded bench surface and the technicians should ground themselves prior to handling devices. This is done most effectively by having the technician wear a conductive wrist strap in series with 100 k ohms to ground. (Motorola ST1191 Wrist Strap is recommended.)

c. Nylon clothing should not be worn while handling MOS circuits.

d. Do not insert or remove MOS devices with power applied. Check all power supplies to be used for testing MOS devices and be certain there are no voltage transients present.

e. When lead straightening, provide ground straps for the apparatus used.

f. When soldering, use a grounded soldering iron.

g. All power should be turned off in a system before printed circuit boards containing MOS devices are inserted or removed.

h. All printed circuit boards containing MOS devices should be provided with shorting straps across the edge connector when being carried or transported.

i. MOS devices should be handled by their packages and not by the leads, if at all possible. Prior to touching the unit, the technician should touch an electrical ground to remove any static charge that may have accumulated. The package and substrate may be electrically common. If so, the reaction of a discharge to the case would cause the same damage as touching the leads.

2. RADIO CIRCUIT BOARD REPAIR

The four-layer radio circuit board presents some new considerations when soldering and unsoldering components. The printed through holes may interconnect two, three, or all four layers of printed circuit. Care should be exercised to avoid pulling the plated circuit out of the hole. If parts under the flex circuit must be replaced, it may be necessary to unsolder part of the flex circuit covering the desired area on the circuit board. Refer to the following paragraph regarding flexible circuits.

When soldering near the module socket pins, use care to avoid accidently getting solder in the guide pin socket, which is open on the end. Insert the module pusher tool into the hole while soldering. Also, be careful not to form solder bridges between module socket pins. Inspect your work for shorts due to solder bridges.

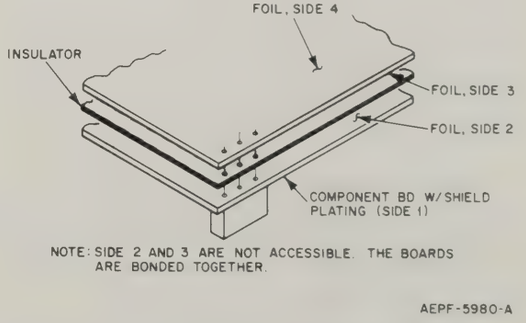

FOIL, SIDE 4
INSULATOR
FOIL, SIDE 3
FOIL, SIDE 2
COMPONENT BD W/SHIELD PLATING (SIDE 1)
NOTE: SIDE 2 AND 3 ARE NOT ACCESSIBLE. THE BOARDS ARE BONDED TOGETHER.
AEPF-5980-A

Figure 38. Typical Four-Layer Board Construction

3. FLEXIBLE CIRCUIT REPAIR

a. General

NOTE

To remove the flex circuit from the radio frame it is not necessary to unsolder socket J302. This socket plugs into the pins on the external accessory connector and can be removed by gently prying it apart.

The flexible circuits are made from a different material than the rigit circuit board and different techniques must be used when soldering.

Excessive prolonged heat on the flexible circuit can damage the material. Avoid excessive heat and excessive bending.

For parts replacement, use the ST1087 Temperature Controlled Solder Station with a 600° or 700° tip, and use small diameter solder such as ST633. The smaller size solder will melt faster and require less heat applied to the circuit.

b. Removing Flex Circuits from Radio Circuit Board

Use care when unsoldering a flex circuit from the radio printed circuit board. The ST1144 Soldering Iron with the large reservoir tip, Part No. 6684208D37 is recommended for this operation. Use the ST1146 Stand to hold the soldering iron. For best results keep the reservoir tip full of solder and the solder skimmed clean.

c. Removing Parts on Radio Control Flex

To replace a part on the radio control flex circuit, such as a volume control or frequency switch, grasp the edge of the flex circuit near the part to be removed with seizers and pull gently. Apply the tip of the soldering iron to the component connections while pulling with the seizers. Do not attempt to puddle out components off the control flex circuit. Prolonged heat applied to the flex circuit may cause damage.

d. Replacing Fuse Clips on Power Flex Circuit

The fuse clips are small and difficult to align properly in the flex circuit prior to soldering. The following procedure uses the radio housing as an alignment fixture.

(1) Remove the bottom of the power flex circuit as described in the disassembly section of this manual.

(2) Unsolder the old fuse clips and clean the holes.

(3) Temporarily place a piece of adhesive tape over the clip holes on the soldered (top) side of the flex circuit.

(4) Insert the fuse clips (from the bottom side) into the holes in the flex circuit with the tabs on the clips towards the outside edges of the flex circuit.

(5) Position the flex circuit in the housing and press the fuse clips into the holes in the housing until they snap in place.

(6) Remove the tape from the clip holes.

(7) Carefully solder the fuse clips to the flex circuit.

CAUTION

Avoid excessive or prolonged heat to prevent melting the radio housing.

(8) If a new power flex circuit is being installed, solder the threaded battery contact studs to the flex circuit at this time.

4. REPLACING THE TOP ESCUTCHEON

a. Removing the Old Escutcheon

(1) Unscrew the antenna from the antenna bushing.

(2) Remove the knobs and retaining nuts on any controls that are mounted through the escutcheon.

(3) At the outside corner, next to the antenna bushing, carefully lift the edge of the escutcheon with a sharp instrument such as a small jewelers screwdriver.

(4) Carefully pry up the old escutcheon.

b. Installing New Escutcheon

The new escutcheon is supplied with a piece of two-sided adhesive which must be first attached to the escutcheon. Proceed as follows:

(1) Remove the paper backing from the side of the adhesive strip that will attach to the under side of the escutcheon.

(2) Carefully position the adhesive strip in place on the under side of the escutcheon.

(3) Remove the paper backing from the other side of the adhesive strip now affixed to the escutcheon.

(4) Carefully position the escutcheon in place over the controls and press firmly in place.

(5) Replace the antenna, control nuts, and control knobs as applicable.

5. REPLACING CONTROLS

a. General

Most of the operating controls are attached to the radio control flex. First remove the battery and disassemble the data terminal section, back cover, and radio circuit board, as previously described under "Disassembly Procedures."

b. Volume Control

(1) Remove the knob and retaining nut from the top of the control.

(2) Unsolder the two wires connecting the power flex to the switch on the control.

(3) Carefully fold the power flex back from the control to obtain working room.

(4) Carefully unsolder the control from the flex circuit at three points.

(5) Lift the volume control out and replace.

c. Squelch Control

(1) Remove the knob from the control.

(2) Carefully remove the escutcheon as described in this section (paragraph 4).

(3) Remove the retaining nut from the top of the control.

(4) Carefully unsolder the flex circuit tab from the control and fold the tab away from the control.

(5) Remove the control and replace.

d. Transmit Indicator LED

(1) Carefully remove the escutcheon as explained in this section.

(2) Unsolder the two leads from the control flex.

(3) Remove the LED from the top of the radio section.

(4) Insert the new LED into the holes from the top of the radio. Observe the polarity markings on the control flex.

(5) Solder the new LED in place and replace the escutcheon.

e. Push-To-Talk Switch

(1) Carefully pry off the protective boot and actuator.

(2) Remove the two exposed screws under the boot and actuator.

(3) Inside the radio, pry off the white strain relief that holds the flex circuit against the frame.

(4) Unsolder the flex circuit from the switch and fold the flex circuit back to remove the switch.

f. Accessory Connector on Side of Radio

(1) Remove the indicator LED as previously explained in paragraph d.

(2) Remove the push-to-talk switch boot and actuator and the strain relief as previously described in steps (1) - (3) of paragraph e.

(3) Fold the flex circuit inward to obtain access to the connector.

(4) Carefully unsolder the connector from the flex circuit.

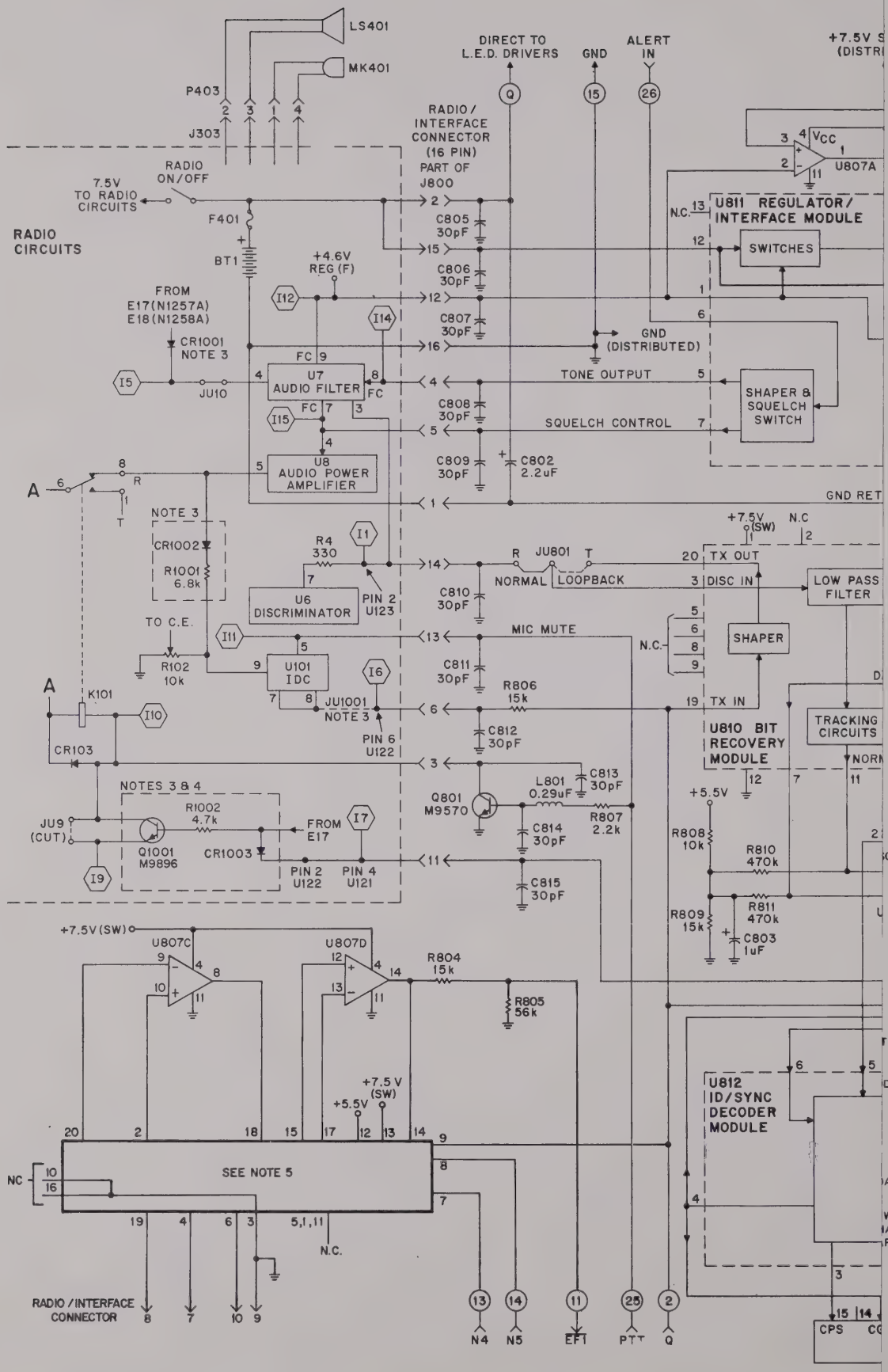


Figure 39. NLN4995A Data Terminal Interface Board Schematic Diagram

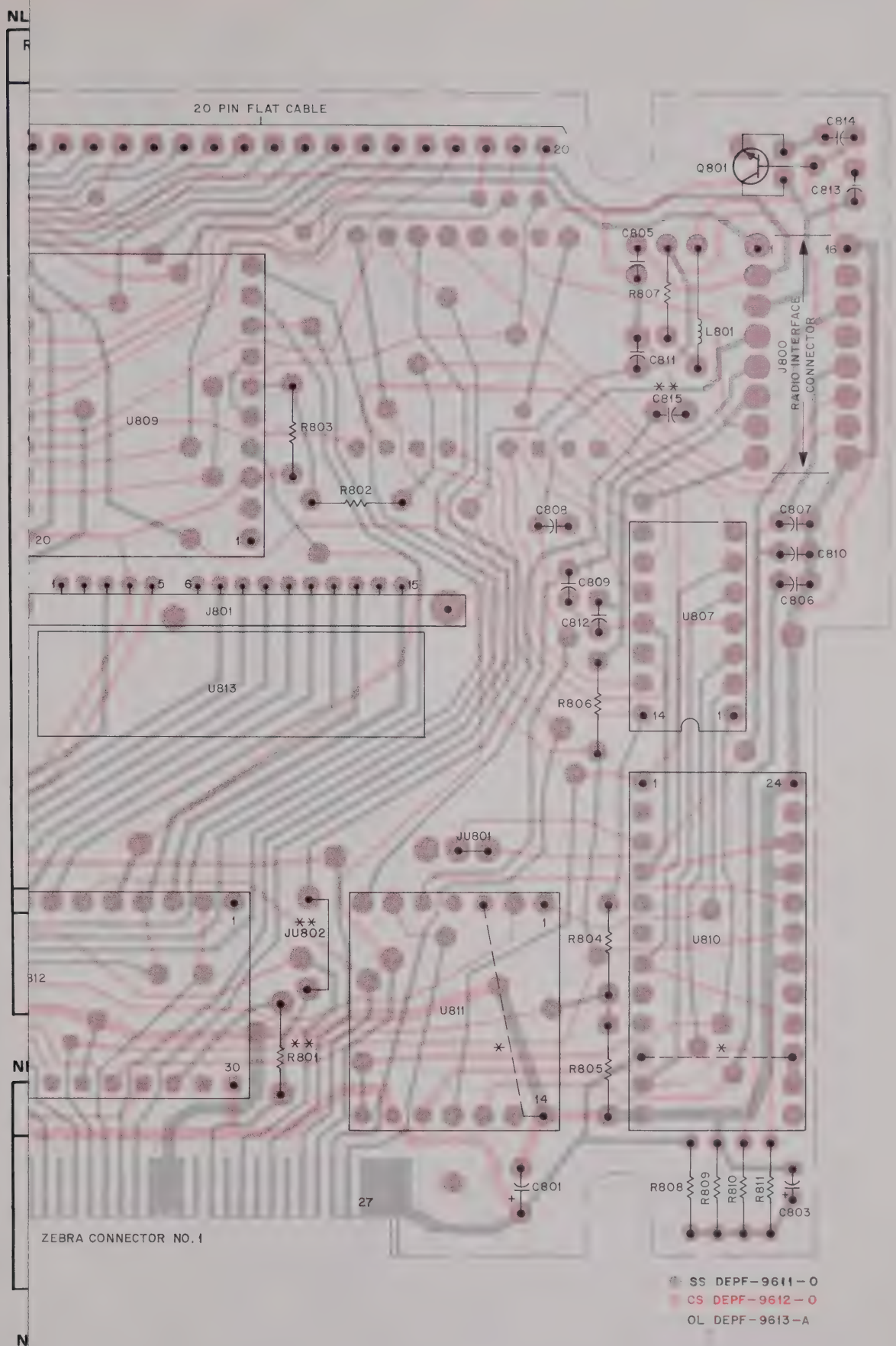
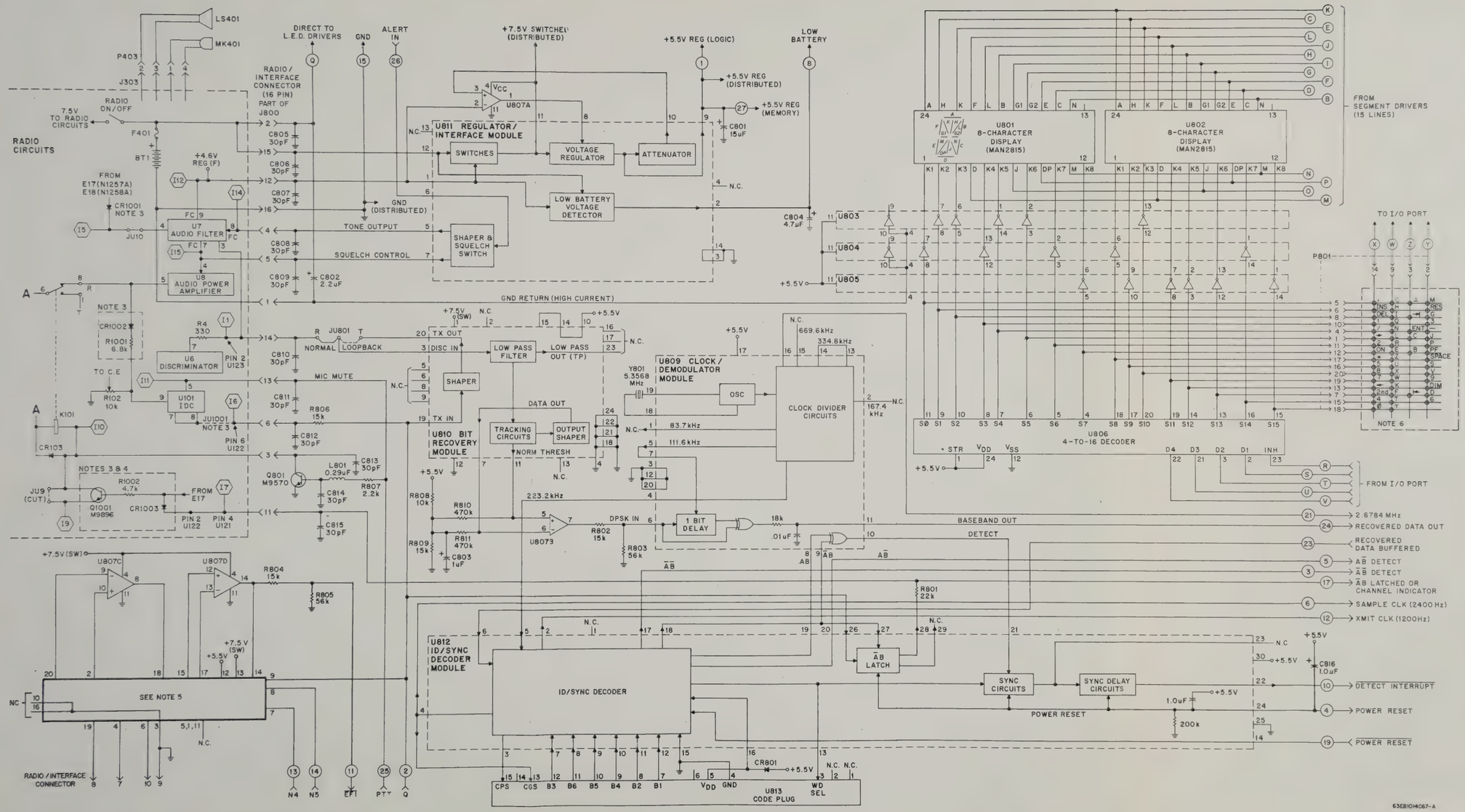


Figure 40. NLN4995A Data Terminal Interface Board Component Layout Diagram and Parts List



NOTES:

1. CONNECTIONS BETWEEN THIS BOARD AND PROCESSOR BOARD ARE AS FOLLOWS:
   - N.C. — 22 — 20 — 18 — 18
   - N.C. — A — 7 — 9
   - ZEBRA CONNECTOR NO. 1: 1 — 27
   - ZEBRA CONNECTOR NO. 2: A — Z
2. ⬡ INDICATES CONNECTION POINT TO INTERCONNECT FLEXIBLE CIRCUIT.
3. THESE PARTS MOUNTED ON BACK OF RADIO BOARD.
4. Q1001, R1002, & CR1003 USED ON 2-FREQUENCY MODEL (N1258A) ONLY.
5. NOT USED
6. KEY BOARD MATRIX (ONLY 1ST FUNCTION SHOWN). "SPACE" CONTAINS 2 KEYS IN PARALLEL (COMMON MATRIX POINT).
   ⊕ = —o—o— (N/O SWITCH)
7. CAPACITOR C816 SHOULD BE ADDED TO ALL P.C. BOARDS THAT DO NOT HAVE IT.
8. IF MODULE U811 IS REPLACED BY ANOTHER U811 WITH REVISION "3" NUMBER OR HIGHER, CAPACITOR C804 MUST BE CHANGED TO A 4.7 uF VALUE; IF IT IS NOT ALREADY THAT VALUE, SEE PARTS LIST. OBSERVE POLARITY DURING REPLACEMENT.

EPF 10282-0

Figure 39. NLN4995A Data Terminal Interface Board Schematic Diagram

NLN4995A Interface Board PLF-1491-A

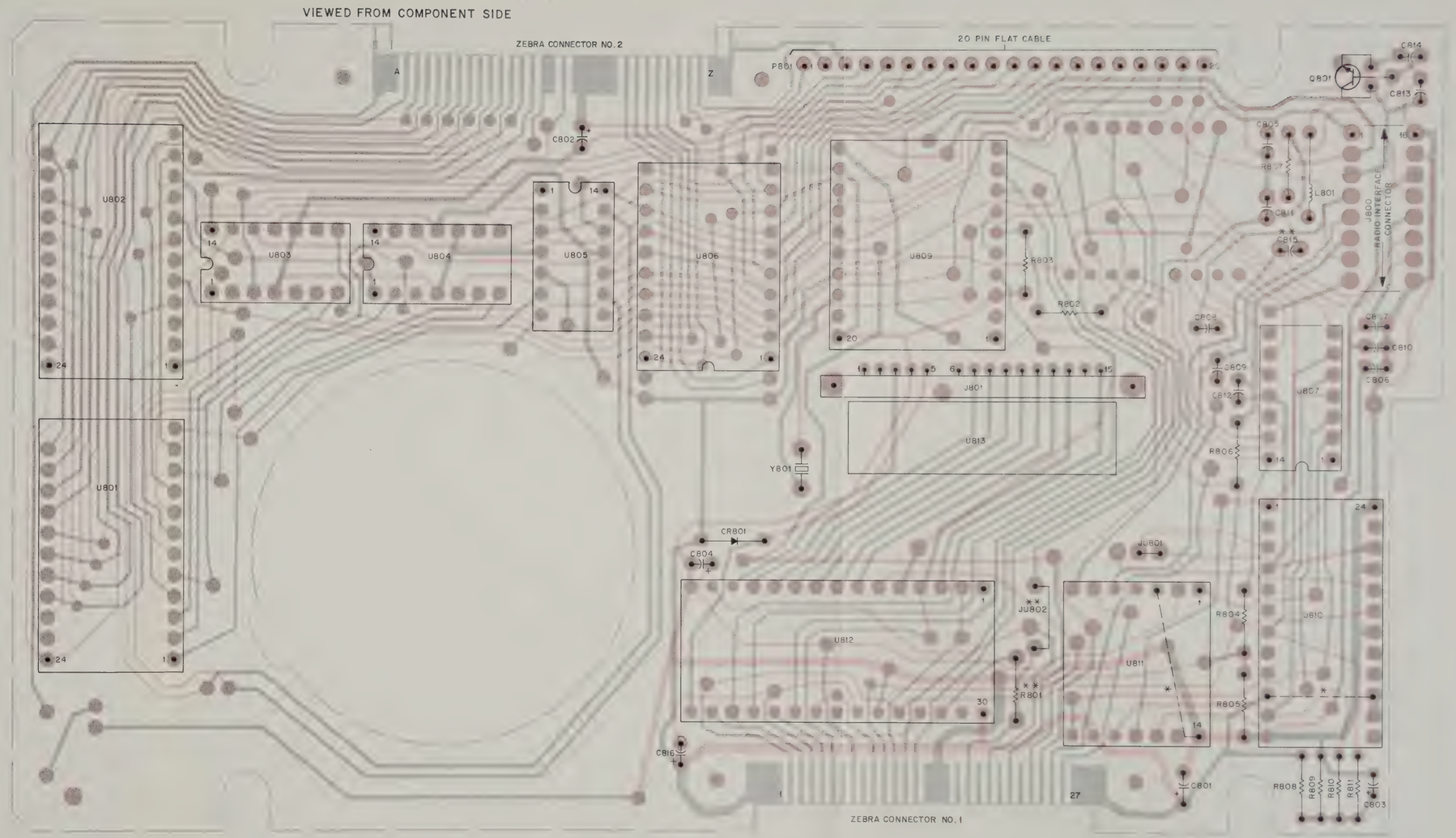
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±20%; 10 V unless stated
C801	2382397D04	15; 15 V
C802	2382397D19	2.2
C803, 816	2382397D07	1.0; 20 V
C804	2383441B18	4.7; 20 V
C805 thru 815	2182358G95	30 pF ±10%; 75 V; N750
CR801	4882363E03	DIODE: See Note I Silicon
		JACK:
J801	0905742F01	Socket, right angle code plug
L801	2482723H04	COIL, RF: unless stated Choke, 0.29 uH
P801	0105950E55	PLUG: Cable, Flat ribbon
Q801	4800869570	TRANSISTOR: See Note I NPN; type M9570
		RESISTOR, Fixed: Ω ±5%; 1/8 W unless stated
R801	0600185A81	22 k
R802	0600185A77	15 k
R803	0600185A91	56 k
R804	0600185A77	15 k
R805	0600185A91	56 k
R806	0600185A77	15 k
R807	0600185A57	2.2 k
R808	0600185A73	10 k
R809	0600185A77	15 k
R810, 811	0600185B14	470 k
		INTEGRATED CIRCUIT:
U801, 802	5105192E07	8-Character Display
U803, 804, 805	5184688D38	Display Driver, type SN75492N
U806	5184887K72	CMOS; Decoder
U807	5184621K69	Operational Amplifier
U809	5105192E09	Hybrid, Clk/Demodulator
U810	5105192E10	Hybrid, Bit Recovery
U811	5105192E11	Hybrid, Regulator/Interface
U812	5105192E12	Hybrid, ID Sync/Decoder
U813	NLN4701A	Code Plug (Programmed)
		CRYSTAL, Quartz: See Note II
Y801	4805664G02	Resonator
NONREFERENCED ITEMS		
	0105950E54	BOARD, P.C.
	0705196A01	BOOT, Crystal
	4505888G01	CONNECTOR PULLERS
	0905287C06	SOCKET, Solder Type (19 ea.)
	0505758B03	EYELET, Code Plug Socket (2 ea.)

NLN5390A 2-Freq. Option Kit PLF-1493-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
Q1001	4800869896	TRANSISTOR: See Note NPN; type M9896
R1002	0600185A65	RESISTOR, Fixed: Ω 4.7 k ±5%; 1/8 W
CR1003	4882363E03	DIODE: See Note Silicon

NLN5389A Data Squelch Circuit PLF-1495-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
CR1001, 1002	4882363E03	DIODE: See Note Silicon
R1001	0600185A69	RESISTOR, Fixed: Ω 6.8 k ±5%; 1/8 W

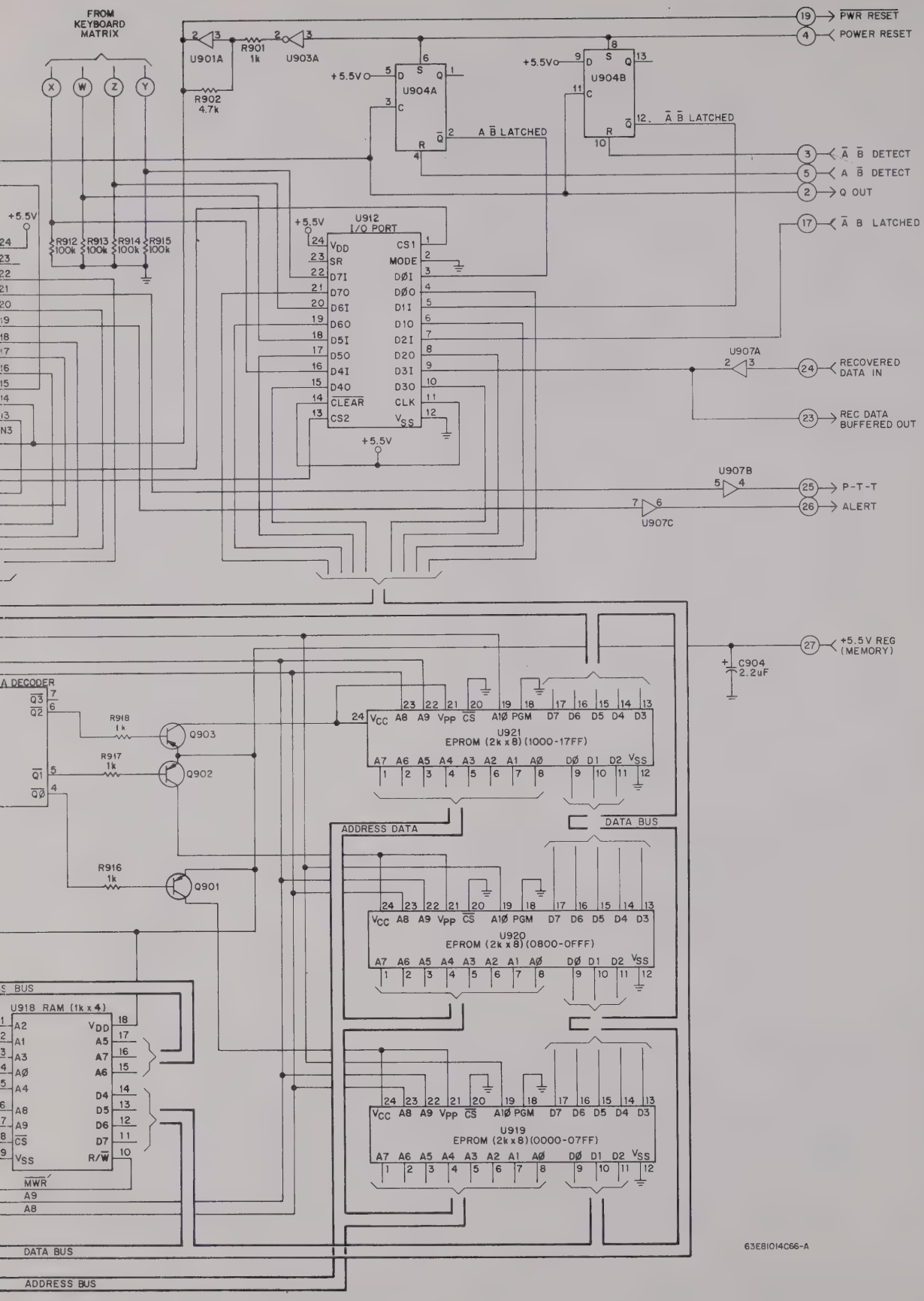


NOTES:

I. For optimum performance, order replacement diodes and transistors by Motorola part number only.

II. When ordering crystal units, specify carrier frequency(s), crystal frequency(s), and crystal type number. Proper oscillator frequency and crystal type will be found stamped on crystal can.

Figure 40. NLN4995A Data Terminal Interface Board Component Layout Diagram and Parts List



64 *Figure 41. NLN4992A Data Terminal Processor Board Schematic Diagram*

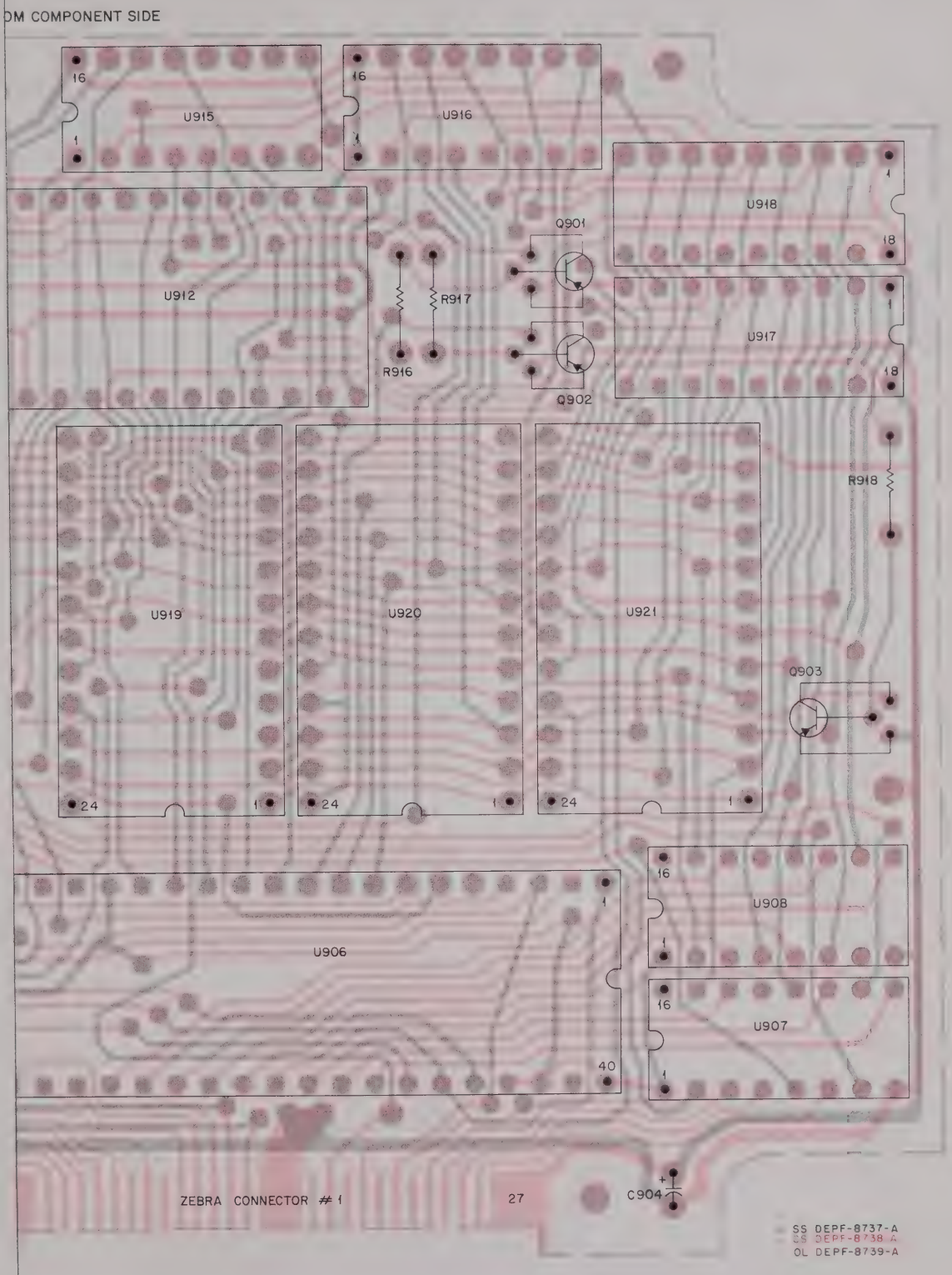
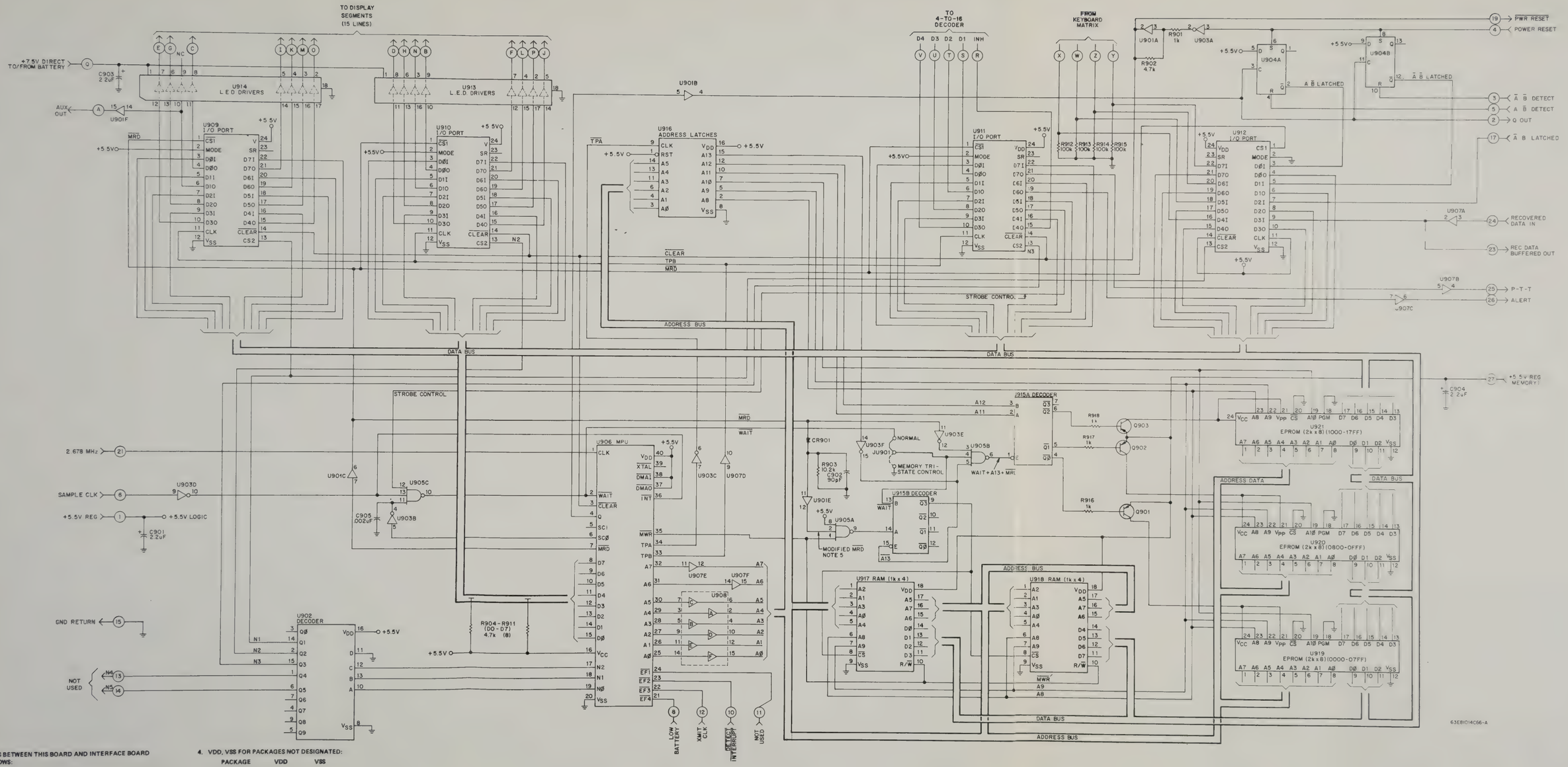


Figure 42. NLN4992A Data Terminal Processor Board Component Layout Diagram and Parts List



NOTES:

1. CONNECTIONS BETWEEN THIS BOARD AND INTERFACE BOARD ARE AS FOLLOWS:
   ZEBRA CONNECTOR 1 = (1) → (27) (7, 9, 16, 18, 20, 22 NOT USED)
   ZEBRA CONNECTOR 2 = (A) → (Z)
2. N.C. (NO CONNECTION)
3. CIRCUITS NOT USED

9 10 U901D

4. VDD, VSS FOR PACKAGES NOT DESIGNATED:

PACKAGE	VDD	VSS
U901	PIN 1	PIN 8
U903	PIN 1	PIN 8
U904	PIN 14	PIN 7
U905	PIN 14	PIN 7
U907	PIN 1	PIN 8
U908	PIN 1	PIN 8
U915	PIN 16	PIN 8

5. MODIFIED $\overline{MRD}$ IS DERIVED FROM $\overline{MRD}$ AS SHOWN ON TIMING DIAGRAM (FIGURE 17).

EPF-9257-O

Figure 41. NLN4992A Data Terminal Processor Board Schematic Diagram

NLN4992A Processor Board PLF-1488-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±20%; 10 V unless stated
C901	2382397D19	2.2
C902	2100859202	90 pF ±5%; 75 V; N750
C903, 904	2382397D19	2.2
C905	2183162H07	2000 pF ±10%; 50 V; NPO
		DIODE: See Note
CR901	4882363E03	Silicon
		TRANSISTOR: See Note
Q901, 902, 903	4800869760	PNP; type M9760
		RESISTOR, Fixed: Ω ±5%; 1/8 W unless stated
R901	0600185A49	1 k
R902	0600185A65	4.7 k
R903	0683175C93	10.2 k ±1%; 1/4 W
R904 thru 911	0600185A65	4.7 k
R912 thru 915	0600185A97	100 k
R916, 917, 918	0600185A49	1 k
		INTEGRATED CIRCUIT:
U901	5184887K02	CMOS; Buffer type CD4050B
U902	5182822F17	CMOS, Decoder type CD4028AE
U903	5184887K01	CMOS, Inverter type CD4049B
U904	5184887K13	CMOS, Flip-Flop type CD4013B
U905	5182822F15	CMOS, Gate type MC14023CD
U906	5182807K24	CMOS, Microprocessor type CDP1802CD
U907, 908	5184887K02	CMOS, Address Buffer type CD4050B
U909 thru 912	5182807K25	I/O Ports type CDP1852CE
U913, 914	5105192E08	Hybrid, LED Segment Driver
U915	5105461G01	CMOS, Decoder MC14556BCP
U916	5184887K70	CMOS, Flip-Flop MC14174BCP
U917, 918	5105462G03	CMOS, RAM type HM6514-5
U919	0105950E57	EPROM, Programmed
U920	0105950E58	EPROM, Programmed
U921	0105950E59	EPROM, Programmed
NONREFERENCED ITEMS		
	0105950E56	BOARD, Processor
	0905351G01	SOCKET, Solderless (72 ea.)
	0905287C06	SOCKET, Solder Type (3 ea.)
	0500139985	EYELET, Retainer (2 ea.)
	4205739F01	RETAINER, Zebra Strip

NOTE: For optimum performance, order replacement diodes and transistors by Motorola part number only.

NLN5388A Zebra Strip and Clamp Kit PLF-1489-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	2805592J01	CONNECTOR, Zebra Strip
	4205741F01	CLIP, Zebra Strip

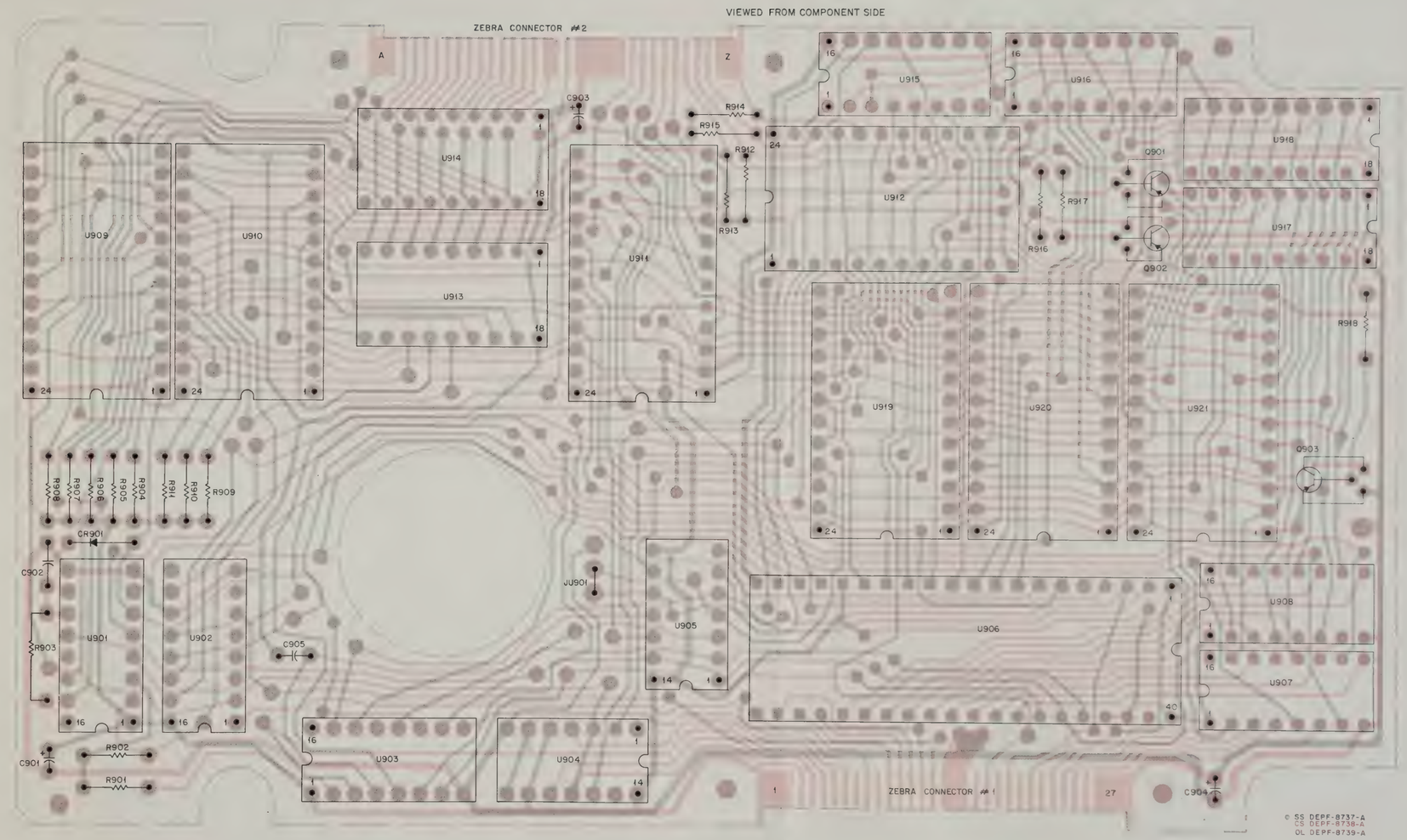
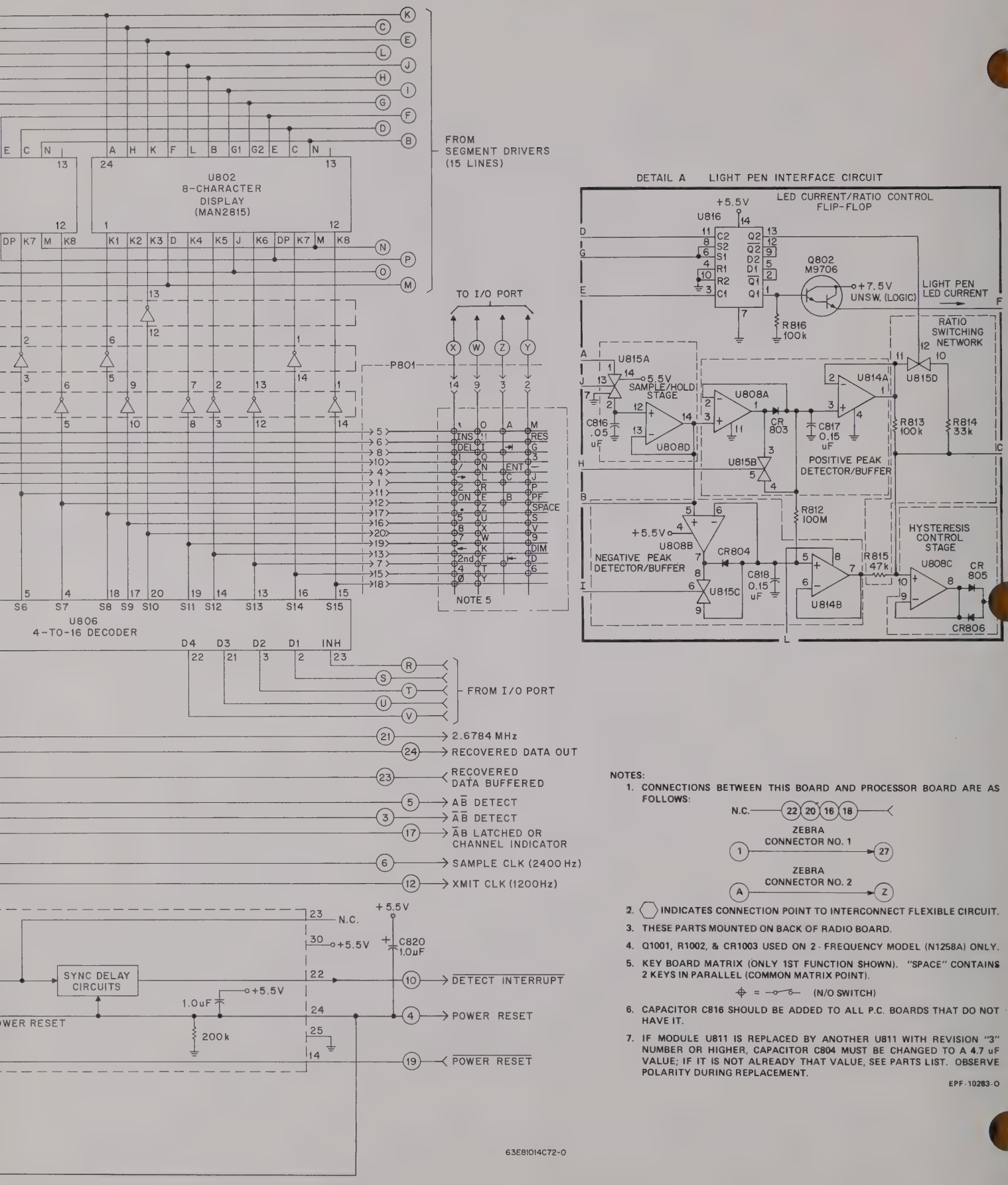


Figure 42. NLN4992A Data Terminal Processor Board Component Layout Diagram and Parts List



63E81014C72-0

NOTES:

1. CONNECTIONS BETWEEN THIS BOARD AND PROCESSOR BOARD ARE AS FOLLOWS:

2. ⬡ INDICATES CONNECTION POINT TO INTERCONNECT FLEXIBLE CIRCUIT.
3. THESE PARTS MOUNTED ON BACK OF RADIO BOARD.
4. Q1001, R1002, & CR1003 USED ON 2-FREQUENCY MODEL (N1258A) ONLY.
5. KEY BOARD MATRIX (ONLY 1ST FUNCTION SHOWN). "SPACE" CONTAINS 2 KEYS IN PARALLEL (COMMON MATRIX POINT).

⊕ = —o o— (N/O SWITCH)

6. CAPACITOR C816 SHOULD BE ADDED TO ALL P.C. BOARDS THAT DO NOT HAVE IT.
7. IF MODULE U811 IS REPLACED BY ANOTHER U811 WITH REVISION "3" NUMBER OR HIGHER, CAPACITOR C804 MUST BE CHANGED TO A 4.7 uF VALUE; IF IT IS NOT ALREADY THAT VALUE, SEE PARTS LIST. OBSERVE POLARITY DURING REPLACEMENT.

EPF-10283-O

Figure 43. NLN7218A Data Terminal Interface Board With Light Pen Circuitry Schematic Diagram

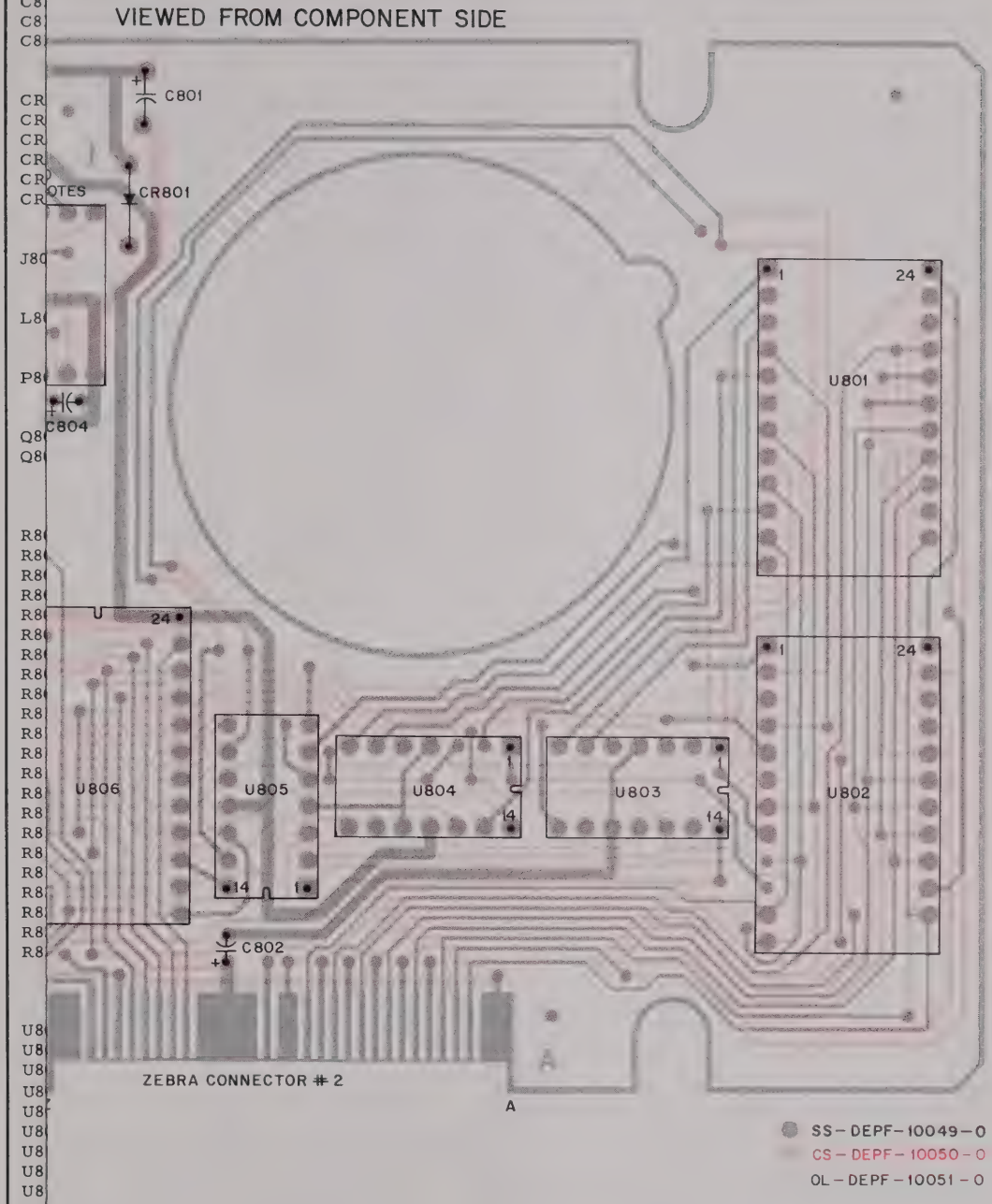
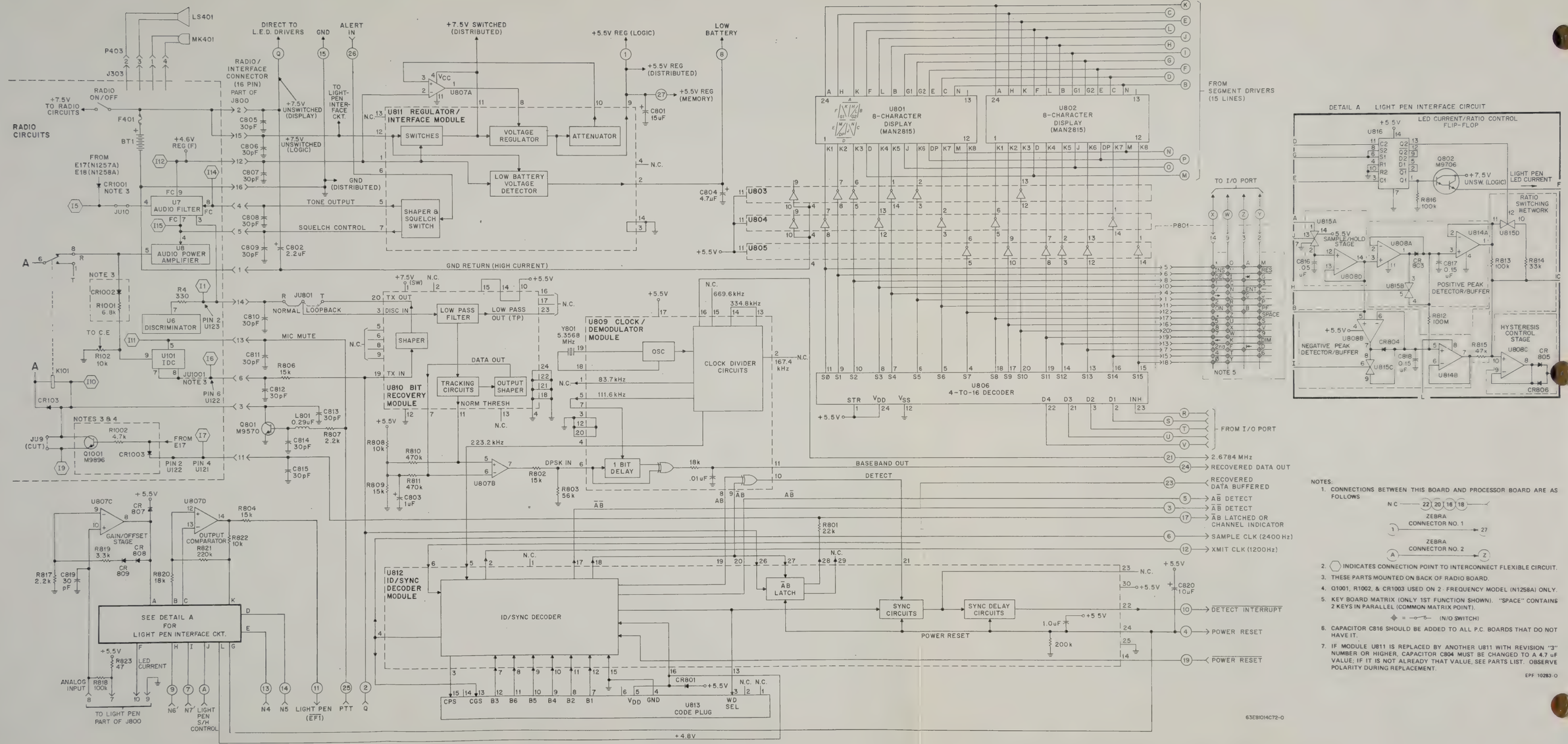


Figure 44. NLN7218A Data Terminal Interface Board With Light Pen Circuitry Component Layout Diagram and Parts Lists



NOTES:

1. CONNECTIONS BETWEEN THIS BOARD AND PROCESSOR BOARD ARE AS FOLLOWS

2. ⬡ INDICATES CONNECTION POINT TO INTERCONNECT FLEXIBLE CIRCUIT.
3. THESE PARTS MOUNTED ON BACK OF RADIO BOARD.
4. Q1001, R1002, & CR1003 USED ON 2 - FREQUENCY MODEL (N1258A) ONLY.
5. KEY BOARD MATRIX (ONLY 1ST FUNCTION SHOWN). "SPACE" CONTAINS 2 KEYS IN PARALLEL (COMMON MATRIX POINT).

◈ = —o—o— (N/O SWITCH)

6. CAPACITOR C816 SHOULD BE ADDED TO ALL P.C. BOARDS THAT DO NOT HAVE IT.
7. IF MODULE U811 IS REPLACED BY ANOTHER U811 WITH REVISION "3" NUMBER OR HIGHER, CAPACITOR C804 MUST BE CHANGED TO A 4.7 uF VALUE; IF IT IS NOT ALREADY THAT VALUE, SEE PARTS LIST. OBSERVE POLARITY DURING REPLACEMENT.

EPF 10283-0

Figure 43. NLN7218A Data Terminal Interface Board With Light Pen Circuitry Schematic Diagram

NLN7218A Interface Board w/Light Pen Circuits PLF-1691-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±20%; 10 V unless stated
C801	2382397D09	6.8
C802	2382397D19	2.2
C803, 820	2382397D07	1.0; 20 V
C804	2383441B18	4.7; 20 V
C805 thru 815	2182358G95	30 pF ±10%; 75 V; N750
C816	2184008H13	0.05; 25 V
C817, 818	2184008H03	0.15; 50 V
C819	2182358G95	30 pF ±10%; 75 V; N750
		DIODE: See Note I
CR801	4882363E03	Silicon
CR802		Not Used
CR803, 804	4882392B09	Silicon
CR805, 806	4883654H01	Silicon
CR807	4884616A01	Hot Carrier
CR808, 809	4883654H01	Silicon
		JACK:
J801	0905742F01	Socket, right angle code plug
		COIL, RF: unless stated
L801	2482723H04	Choke, 0.29 uH
		PLUG:
P801	0105950E55	Connector, right angle
		TRANSISTOR: See Note I
Q801	4800869570	NPN; type M9570
Q802	4800869706	NPN; Darlington type M9706
		RESISTOR, Fixed: Ω ±5%; 1/8 W unless stated
R801	0600185A81	22 k
R802	0600185A77	15 k
R803	0600185A91	56 k
R804	0600185A77	15 k
R805		Not Used
R806	0600185A77	15 k
R807	0600185A57	2.2 k
R808	0600185A73	10 k
R809	0600185A77	15 k
R810, 811	0600185B14	470 k
R812	0605577J01	100 M
R813	0600185A97	100 k
R814	0600185A85	33 k
R815	0600185A89	47 k
R816	0600185A97	100 k
R817	0600185A57	2.2 k
R818	0600185A97	100 k
R819	0600185A61	3.3 k
R820	0600185A79	18 k
R821	0600185B06	220 k
R822	0600185A73	10 k
R823	0600185A17	47
		INTEGRATED CIRCUIT: See Note
U801, 802	5105192E07	8-Character Display
U803, 804, 805	5184688D38	Display Driver, type SN75492N
U806	5184887K72	CMOS; Decoder
U807	5184621K69	Op Amp
U808	5105469E06	Op Amp
U809	5105192E09	Hybrid, Clk/Demodulator
U810	5105192E10	Hybrid, Bit Recovery
U811	5105192E11	Hybrid, Regulator/Interface
U812	5105192E12	Hybrid, ID Sync/Decoder
U813	NLN4701A	Code Plug (Programmed)
U814	5105469E05	Op Amp
U815	5105461G04	CMOS; Analog Switch
U816	5184887K13	CMOS; Dual D F-F
		CRYSTAL, Quartz: See Note II
Y801	4805664G02	5356.800 kHz
NONREFERENCED ITEMS		
	0105957F44	BOARD, P.C.
	0905287C06	SOCKET, Solder Type (19 ea.)
	0505758B03	EYELET, Code Plug Socket (2 ea.)

NKN6259A Ribbon Cable w/Light Pen Connector PLF-1692-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C701	2382397D09	CAPACITOR, Fixed: 6.8 uF ±20%; 10 V
P800	0905547B01	PLUG: Connector
R701, 702	0600185A11	RESISTOR, Fixed: 27 Ω ±5%; 1/8 W
NONREFERENCED ITEM		
	0105957F46	BOARD, Light Pen Connector

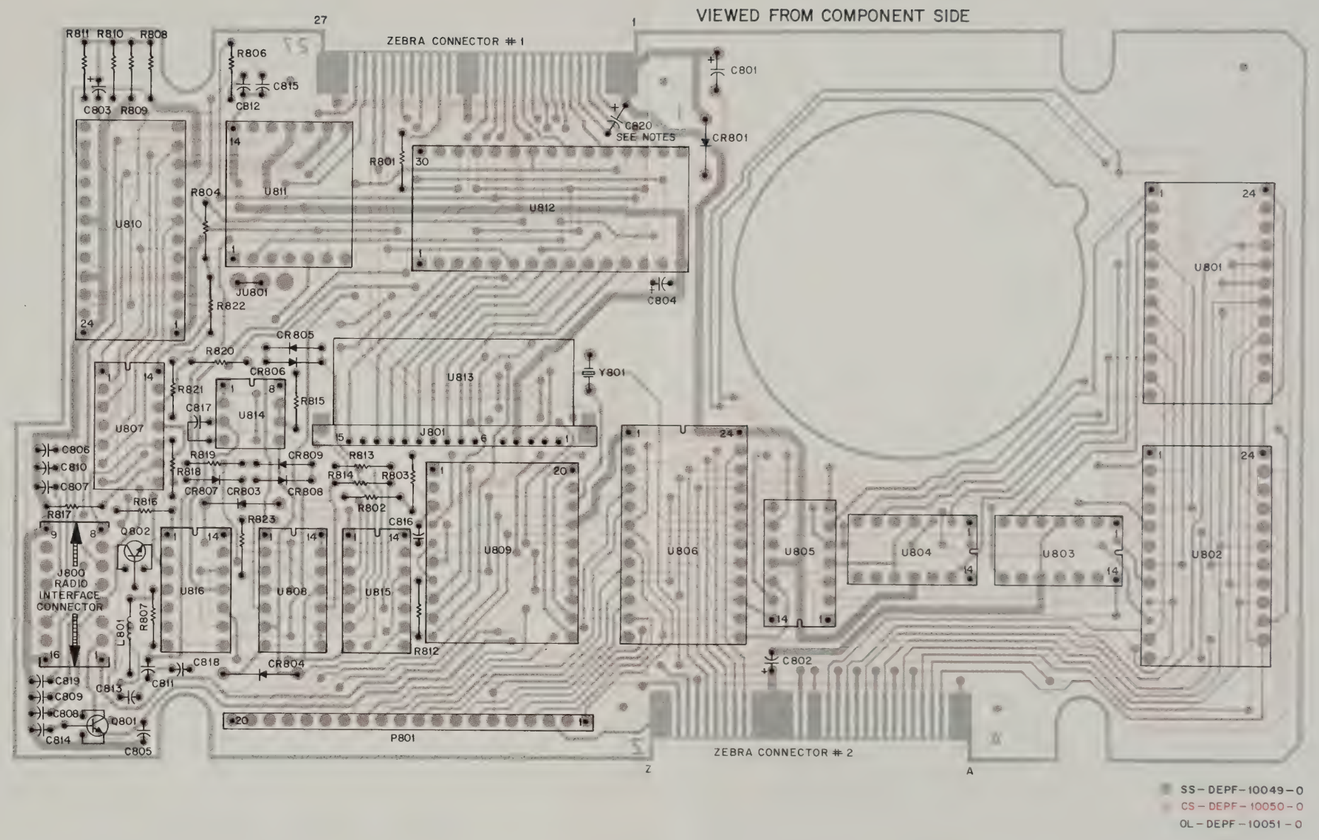
NLN5007A Light Pen w/Cable and Connector PLF-1693-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0105617G01	Light Pen w/Cable and Connector

NLN7221A Light Pen Holder For Standard Case PLF-1694-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	4205779G01	STRAP, Light Pen

NOTES:
I. For optimum performance, order replacement diodes, transistors, and integrated circuits by Motorola part number only.
II. When ordering crystal units, specify carrier frequency(s), crystal frequency(s), and crystal type number. Proper oscillator frequency and crystal type will be found stamped on crystal can.



NOTES:
IF C820 IS TO BE REPLACED, CAPACITOR BODY SHOULD BE POSITIONED BETWEEN +5.5 V RUNNER AND MODULE U812. NOTE THAT CAPACITOR LEADS MUST BE SOLDERED AS DESCRIBED SO AS NOT TO INTERFERE WITH MECHANICAL CLOSURE OF ZEBRA CONNECTOR HOUSING. SOLDER THE POSITIVE (+) CAPACITOR LEAD ON THE COMPONENT SIDE. ENSURE THAT SOLDER DOES NOT DRIP AND OVERFLOW ONTO THE SOLDER SIDE FOIL. CLIP THE LEAD FLUSH WITH THE SOLDER SIDE FOIL. THE NEGATIVE (-) LEAD CAN NOW BE SOLDERED TO THE SOLDER SIDE OF THE BOARD. FOLD THE CAPACITOR FLAT TOWARDS MODULE U811.
EPF 10264-O

Figure 44. NLN7218A Data Terminal Interface Board With Light Pen Circuitry Component Layout Diagram and Parts Lists

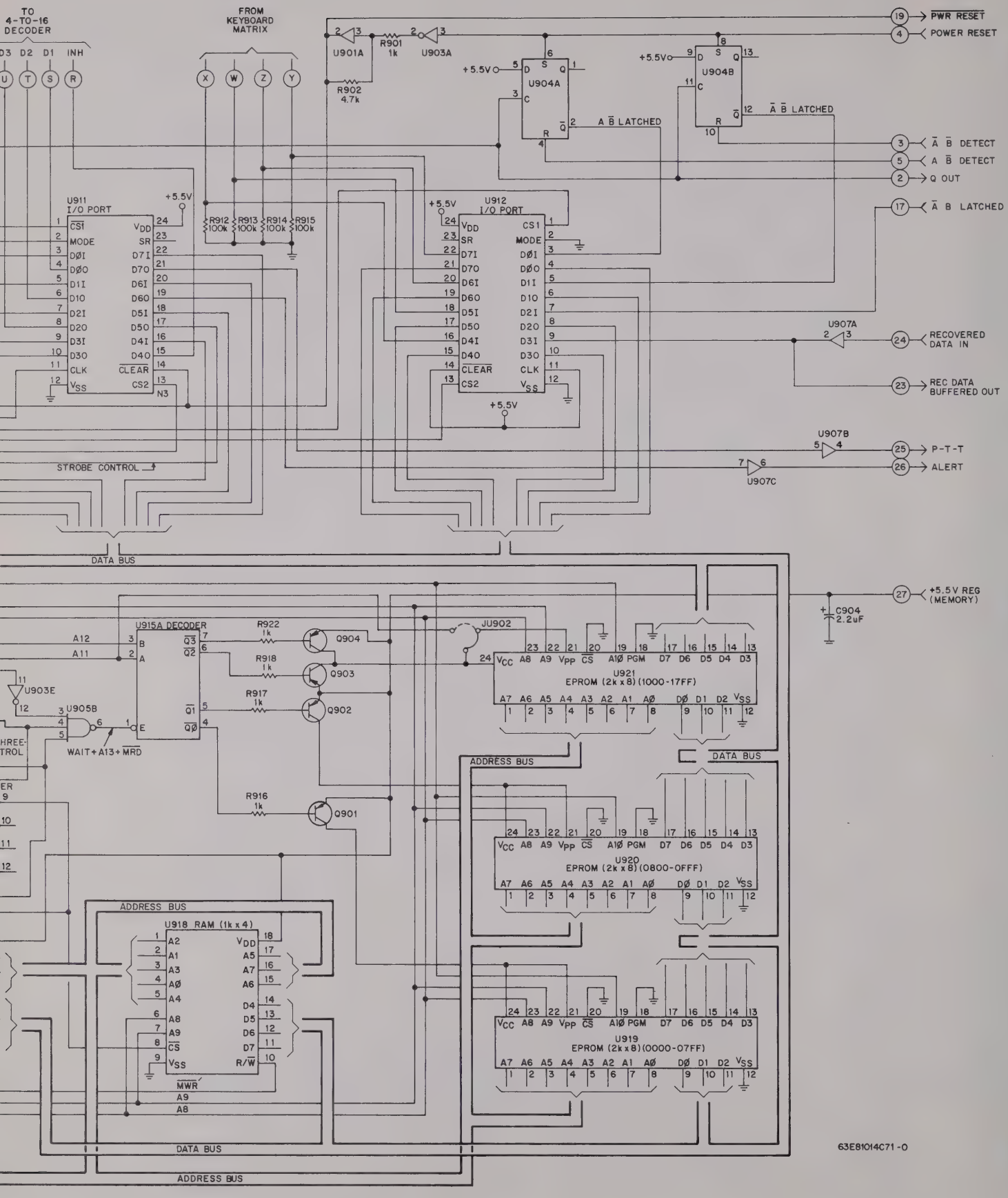


Figure 45. NLN7219A Data Terminal Processor Board With Light Pen Circuitry Schematic Diagram

NLN7219A Processor Board w/Light Pen Circuits

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTIO
		CAPACITOR, Fixed:
		10 V unless stated
C901	2382397D19	2.2
C902	2100859202	90 pF ±5%; 75 V; N7
C903, 904	2382397D19	2.2
C905	2183162H07	2000 pF ±10%; NPO
C906, 907	2182358G94	100 ±10%; 75 V; N22
		DIODE: See Note
CR901	4882363E03	Silicon
CR902, 903	4883654H01	Silicon
		TRANSISTOR: See
Q901, 902, 903, 904	4800869760	PNP; type M9760
		RESISTOR, Fixed:
		unless stated
R901	0600185A49	1 k
R902	0600185A65	4.7 k
R903	0683175C93	10.2 k ±1%; 1/4 W
R904 thru 911	0600185A65	4.7 k
R912 thru 915	0600185A97	100 k
R916, 917, 918	0600185A49	1 k
R919, 920	0600185B27	1.6 M
R921	0600185A91	56 k
		INTEGRATED CIRC
		See Note
U901	5184887K02	CMOS; Buffer type
U902	5182822F17	CMOS; Decoder typ
U903	5184887K01	CMOS; Inverter typ
U904	5184887K13	CMOS; Flip-Flop ty
U905	5182822F15	CMOS; Gate type M
U906	5182807K24	CMOS; Microproce
U907, 908	5184887K02	CMOS; Address Bu
		CD4050B
U909 thru 912	5182807K25	I/O Ports type CDP
U913, 914	5105192E08	Hybrid, LED Segm
U915	5105461G01	CMOS; Decoder MC
U916	5184887K70	CMOS; Flip-Flop M
U917, 918	5105462G03	CMOS; RAM type H
NONREFERENCED ITEMS		
	0105957F45	BOARD, Processo
	4205739F01	RETAINER, Zebra
	0905351G01	SOCKET, Solderle
	0905287C06	SOCKET, Solder T
	0500139985	EYELET, Retaine

NLN7220A PROMs, 3 of 9 Coded

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPT
		INTEGRATED CIR
		See Note
U919	0105957F47	EPROM, Program
U920	0105957F48	EPROM, Program
U921	0105957F49	EPROM, Program

NOTE: For optimum performance, order replacem transistors, and integrated circuits by Mot number only.

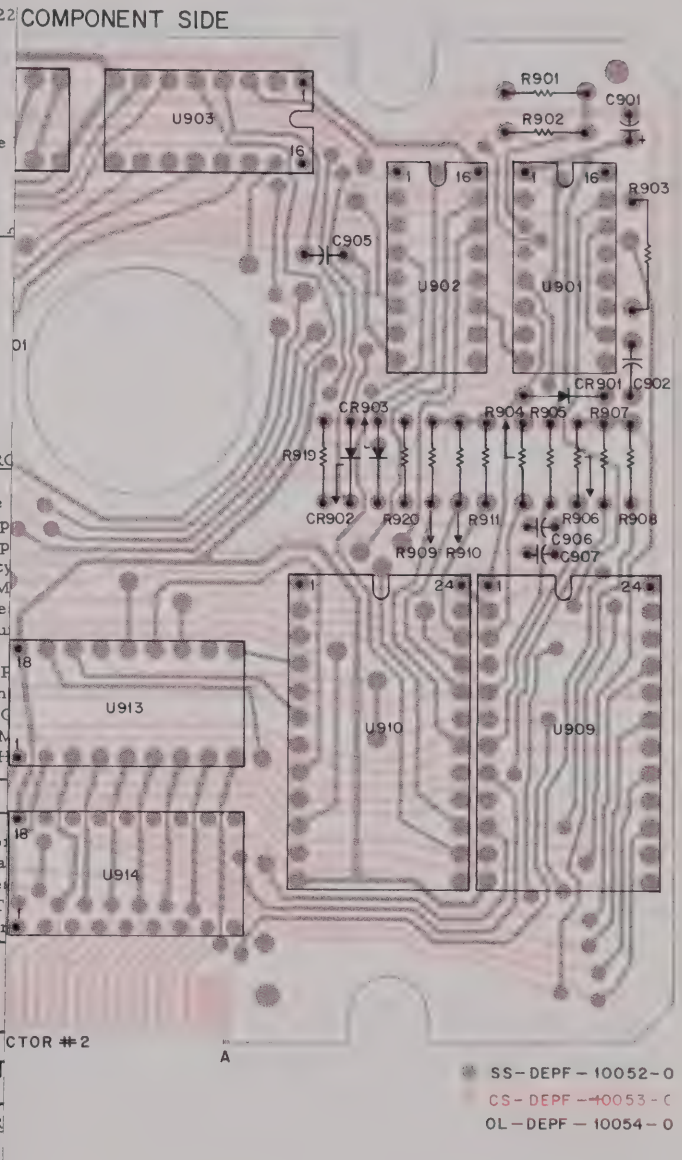


Figure 46. NLN7219A Data Terminal Processor Board With Light Pen Circuitry Component Layout Diagram and Parts Lists

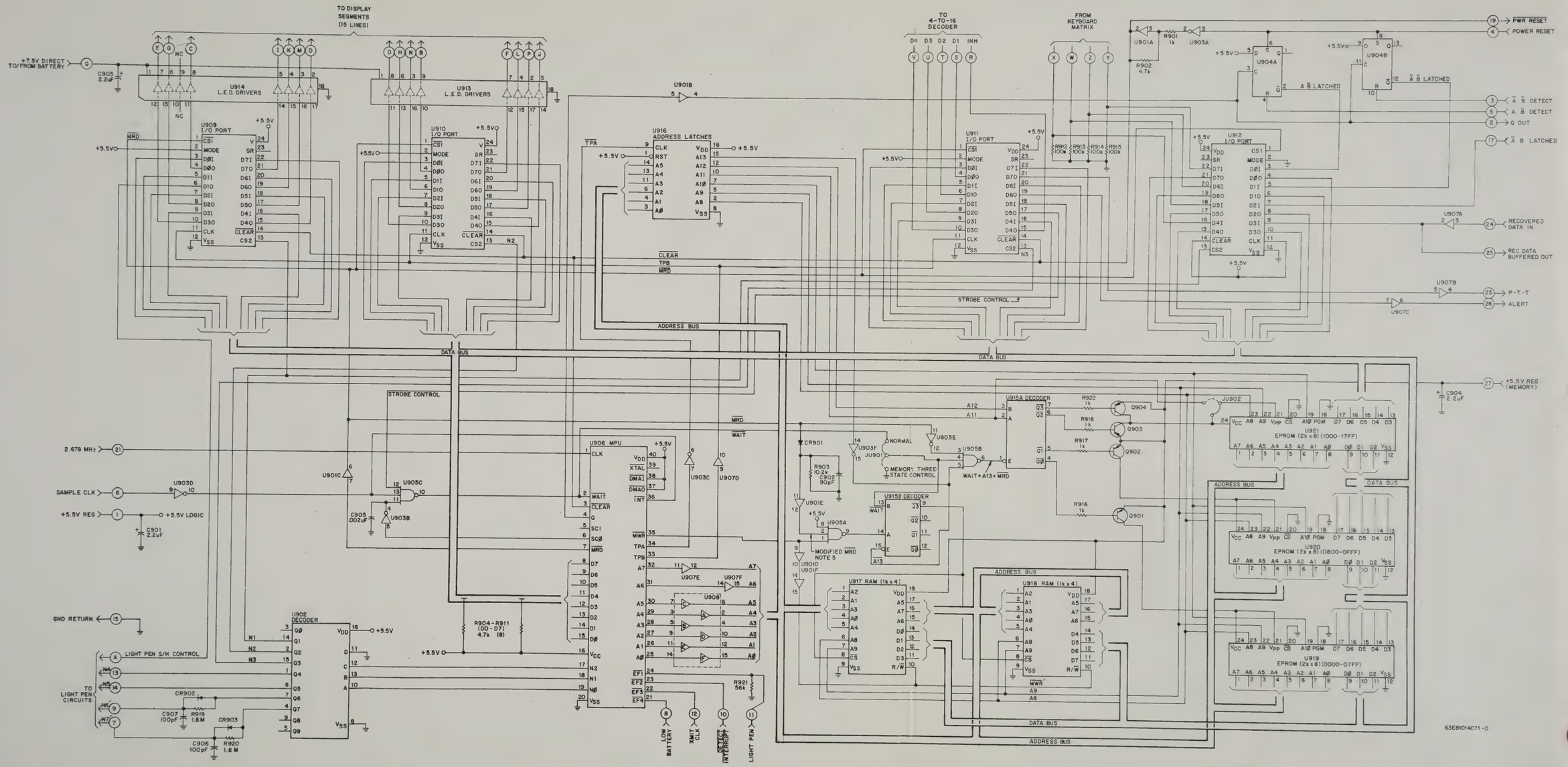


Figure 45. NLN7219A Data Terminal Processor Board With Light Pen Circuitry Schematic Diagram

NLN7219A Processor Board w/Light Pen Circuits PLF-1689-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±20%; 10 V unless stated
C901	2382397D19	2.2
C902	2100859202	90 pF ±5%; 75 V; N750
C903, 904	2382397D19	2.2
C905	2183162H07	2000 pF ±10%; NPO
C906, 907	2182358G94	100 ±10%; 75 V; N2200
		DIODE: See Note
CR901	4882363E03	Silicon
CR902, 903	4883654H01	Silicon
		TRANSISTOR: See Note
Q901, 902, 903, 904	4800869760	PNP; type M9760
		RESISTOR, Fixed: Ω ±5%; 1/8 W unless stated
R901	0600185A49	1 k
R902	0600185A65	4.7 k
R903	0683175C93	10.2 k ±1%; 1/4 W
R904 thru 911	0600185A65	4.7 k
R912 thru 915	0600185A97	100 k
R916, 917, 918	0600185A49	1 k
R919, 920	0600185B27	1.6 M
R921	0600185A91	56 k
		INTEGRATED CIRCUIT: See Note
U901	5184887K02	CMOS; Buffer type CD4050B
U902	5182822F17	CMOS; Decoder type CD4028AE
U903	5184887K01	CMOS; Inverter type CD4049B
U904	5184887K13	CMOS; Flip-Flop type CD4013B
U905	5182822F15	CMOS; Gate type MC14023CD
U906	5182807K24	CMOS; Microprocessor type CDP
U907, 908	5184887K02	CMOS; Address Buffer type CD4050B
U909 thru 912	5182807K25	I/O Ports type CDP1852CE
U913, 914	5105192E08	Hybrid, LED Segment Driver
U915	5105461G01	CMOS; Decoder MC14556BCP
U916	5184887K70	CMOS; Flip-Flop MC14174BCP
U917, 918	5105462G03	CMOS; RAM type HM6514-9
NONREFERENCED ITEMS		
	0105957F45	BOARD, Processor
	4205739F01	RETAINER, Zebra Strip
	0905351G01	SOCKET, Solderless (72 ea.)
	0905287C06	SOCKET, Solder Type (3 ea.)
	0500139985	EYELET, Retainer (2 ea.)

NLN7220A PROMs, 3 of 9 Coded PLF-1690-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		INTEGRATED CIRCUIT: See Note
U919	0105957F47	EPROM, Programmed
U920	0105957F48	EPROM, Programmed
U921	0105957F49	EPROM, Programmed

NOTE: For optimum performance, order replacement diodes, transistors, and integrated circuits by Motorola part number only.

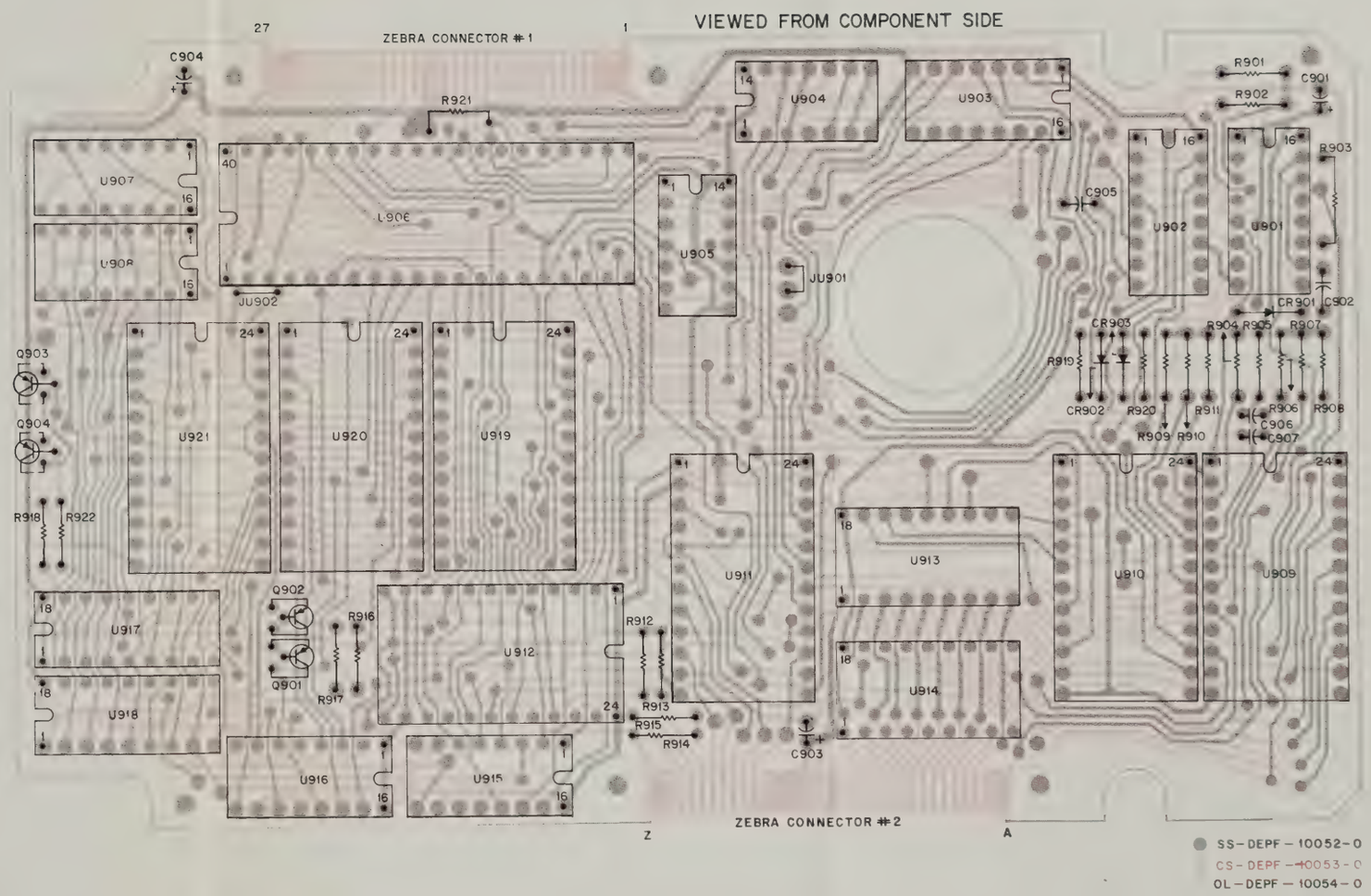
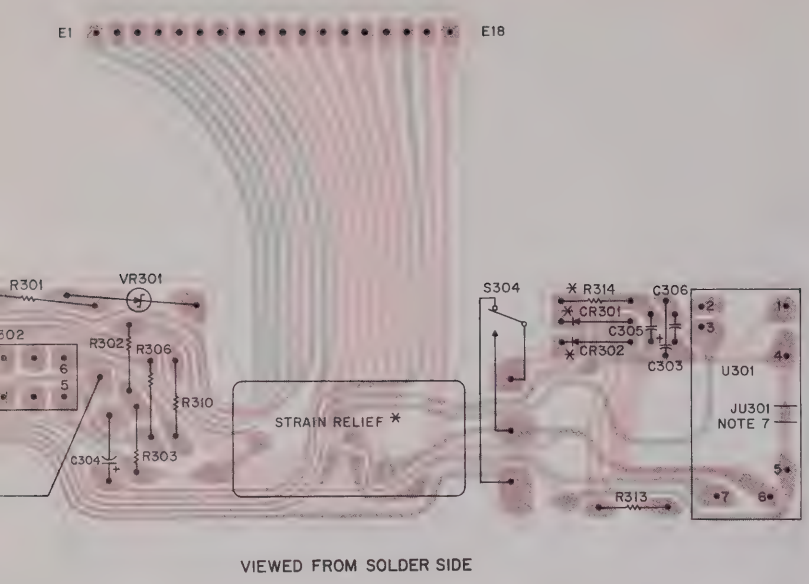


Figure 46. NLN7219A Data Terminal Processor Board With Light Pen Circuitry Component Layout Diagram and Parts Lists

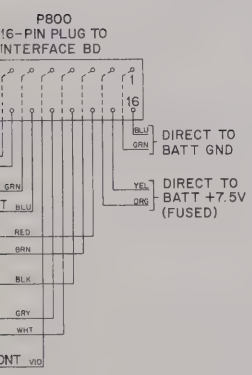


VIEWED FROM SOLDER SIDE

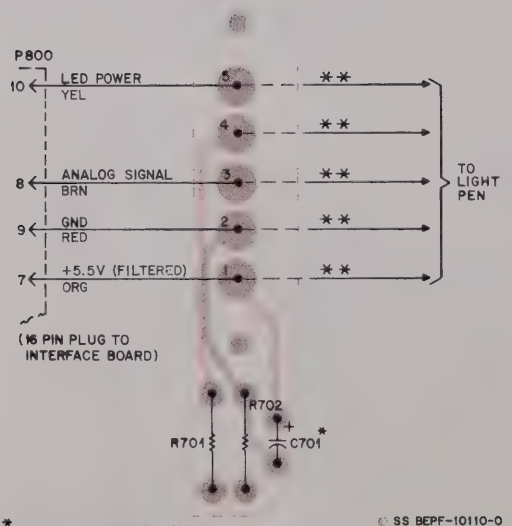
VN UNFOLDED
PARTS MOUNTED ON OTHER SIDE.
ONLY ON 1-FREQ MODELS.
F AT DOTTED LINE ON MULTI-FREQ MODELS.
F AT DOTTED LINE ON 1-FREQ MODELS.
DDELS, THE SQUELCH CONTROL IS LOCATED
WHERE S301 IS NORMALLY MOUNTED.
OUT JU301 WHEN U301 IS USED; C305, C306, AND
NLY WITH U301.
LY ON 2-FREQ MODELS. S501 USED ON
MODELS, ALONG WITH MULTI-FREQ

SOLDER SIDE DEPF-7456-O
COMP SIDE DEPF-7457-O
OL DEPF-7458-D

VIEWED FROM COMPONENT SIDE



SS DEPF-8990-O
OL DEPF-8991-O



*MOUNTED ON SOLDER SIDE
**EXTERNAL CONNECTOR PINS TO LIGHT PEN.

SS BEPF-10110-O
CS BEPF-10111-O
OL BEPF-10112-O

Figure 49. Light Pen Connector (NKN6259A)

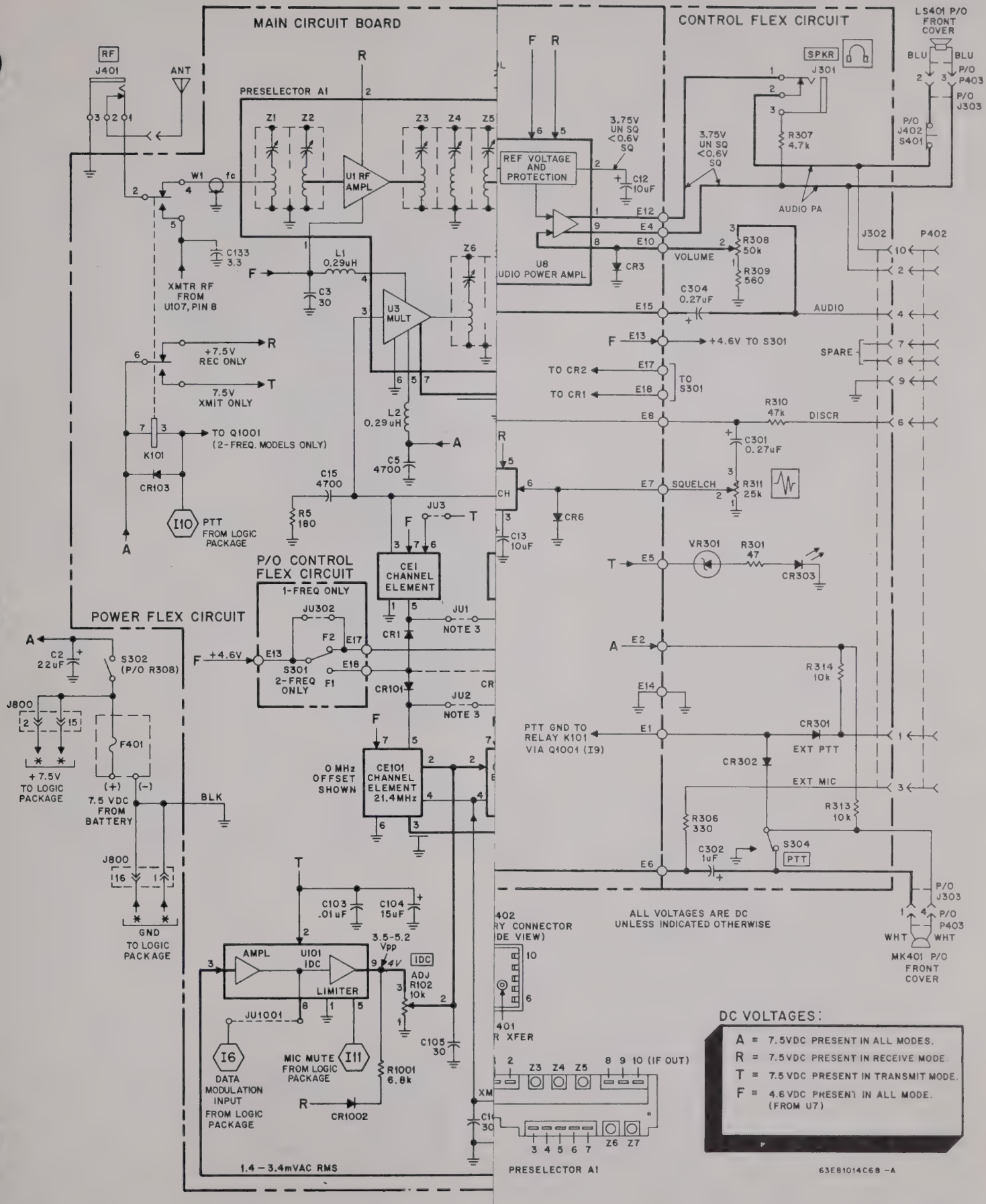
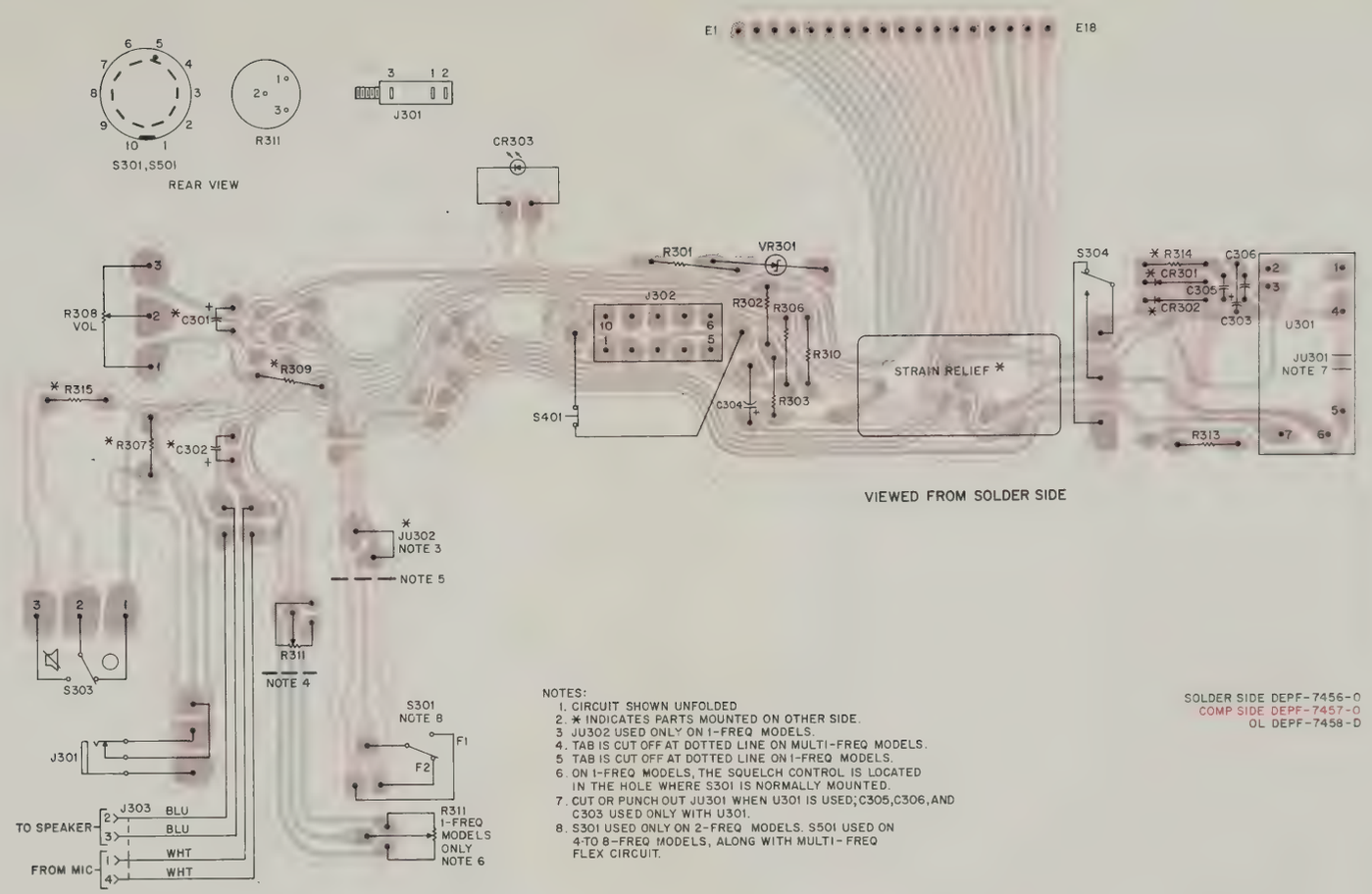


Figure 50. Radio Section, Schematic Diagram



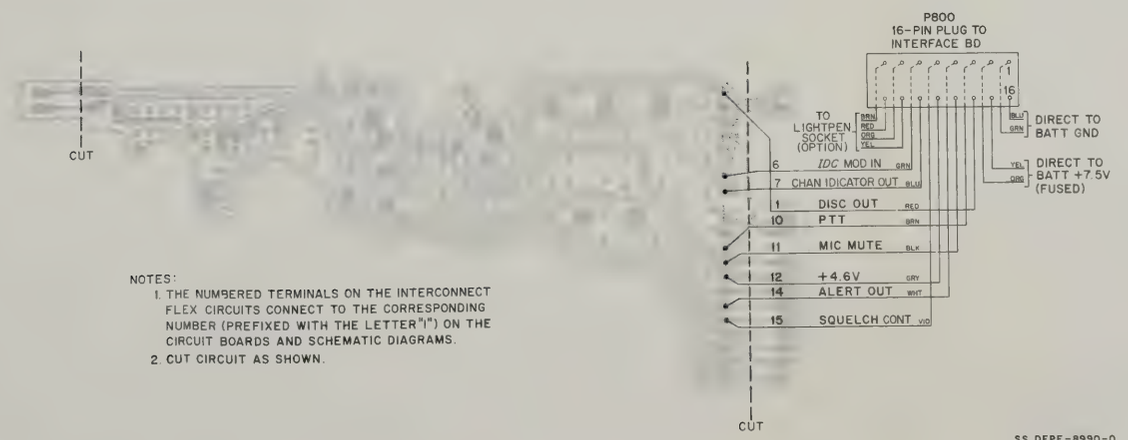


Figure 48. Radio/Terminal Interface, Interconnect Flexible Circuit (NLN5391A)

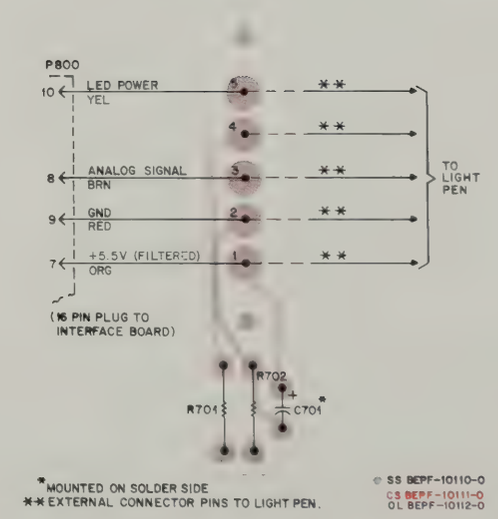
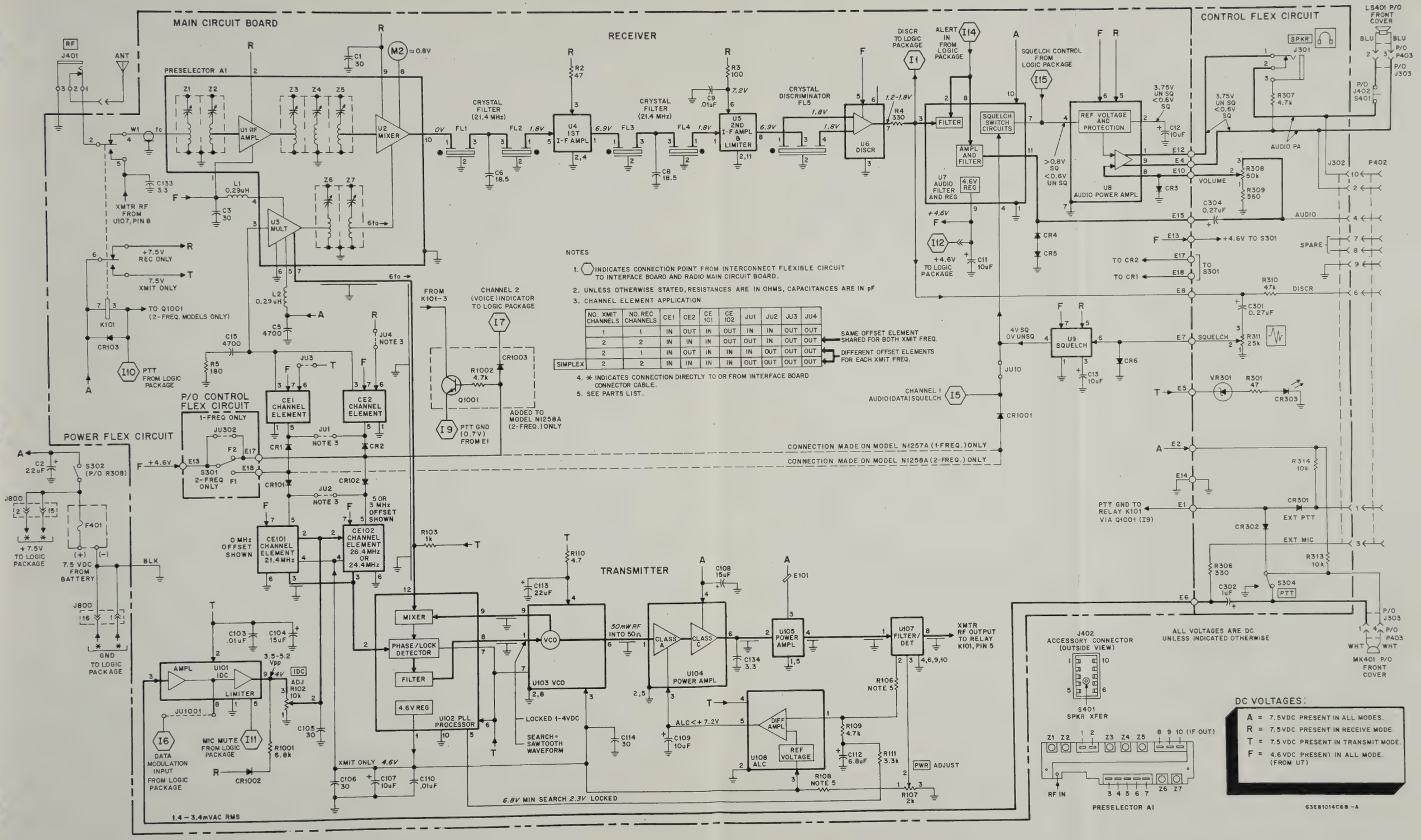


Figure 49. Light Pen Connector (NKN6259A)



NOTES

1. ⬡ INDICATES CONNECTION POINT FROM INTERCONNECT FLEXIBLE CIRCUIT TO INTERFACE BOARD AND RADIO MAIN CIRCUIT BOARD.
2. UNLESS OTHERWISE STATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN pF
3. CHANNEL ELEMENT APPLICATION

	NO. XMIT CHANNELS	NO. REC CHANNELS	CE1	CE2	CE 101	CE 102	JU1	JU2	JU3	JU4	
	1	1	IN	OUT	IN	OUT	IN	IN	OUT	OUT	
	2	2	IN	IN	IN	OUT	OUT	IN	OUT	OUT	← SAME OFFSET ELEMENT SHARED FOR BOTH XMIT FREQ.
	2	1	IN	OUT	IN	IN	IN	OUT	OUT	OUT	← DIFFERENT OFFSET ELEMENTS FOR EACH XMIT FREQ.
SIMPLEX	2	2	IN	IN	IN	IN	OUT	OUT	OUT	OUT	

4. ✳ INDICATES CONNECTION DIRECTLY TO OR FROM INTERFACE BOARD CONNECTOR CABLE.
5. SEE PARTS LIST.

Figure 50. Radio Section, Schematic Diagram

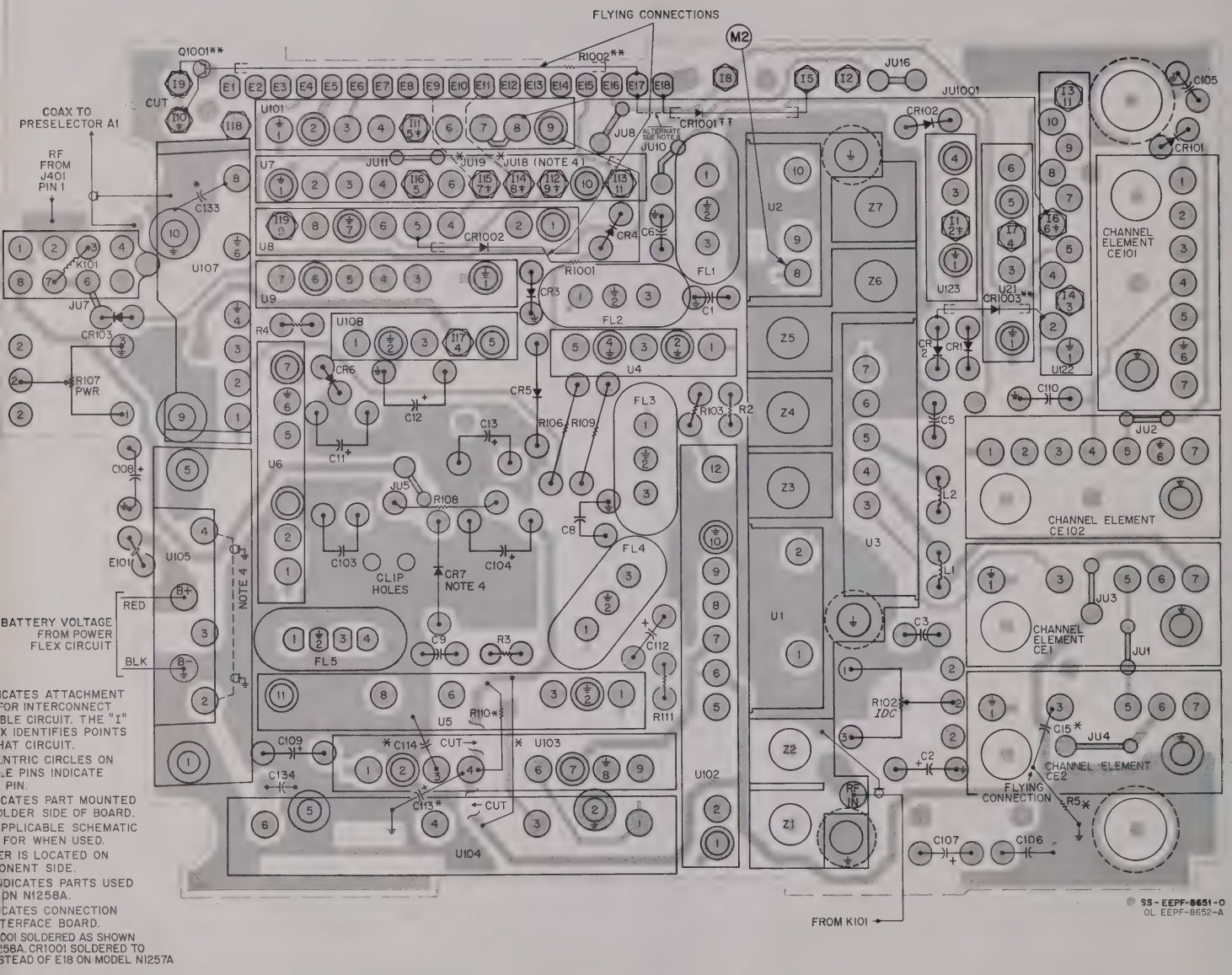


Figure 51. Radio Section, Main Circuit Board Component Layout Diagram and Parts List

APPENDIX A

1. INTRODUCTION

The purpose of this section is to define the three-of-nine (3/9) bar code and to provide a guide for the production of the bar code media. This reference is intended only as a guide, since media quality depends upon the discretion of the ultimate user.

2. MEDIA

a. Contrast Ratio

The contrast ratio of the media depends on the reflectance of the paper (white background) and the density of the print (black bars). Contrast, expressed in terms of the print contrast ratio (PCR), is defined by the following formula:

$$PCR = \frac{\text{Reflectance of Paper} - \text{Reflectance of Bars}}{\text{Reflectance of Paper}}$$

Reflectance must be measured with respect to the light source to be used to read the bar code. In most cases, code 39 will be printed with carbon-based ink, and an infra-red light source used in the pen. Therefore, the reflectometer used to measure the reflectance should use an infra-red filter. A minimum PCR of 0.8 will ensure satisfactory results.

b. Size

Scan rate is to a degree a function of the physical size of the media being scanned. Media, whose widest module (bar or space) is no wider than 0.37 inches, can utilize the full three to thirty inches/second scan rate range of the data terminal. Larger media increases the minimum acceptable scan speed; i.e., modules with a 0.1 inch width require a minimum scan speed of approximately 8 inches/second.

Normal, comfortable scan rates, although subject to individual technique, are usually in the range of 4 to 25 inches/second. Long code strings (many characters in the code line) tend to cause the operator to inadvertently accelerate (double or triple) the scan speed near the end of scan.

c. Three-of-Nine Code Structure (See Figure A1)

This code provides a set of 44 unique combinations (characters) based on nine bits for each character. Three of the nine bits are binary ones and the remainder are zeros. The three-of-nine code is used to sequentially encode an unlimited string of characters. A start/stop character ("*") provides for positive recognition of the beginning and the end of the data string. The start/stop character decodes to an asterisk (Hex ASCII Code 2A) and can be used in the bar coded data string if the asterisk character is desired.

Two fields are used to encode each character, a five-bit field of bars and a four-bit field of spaces. The five-bit bar field uses a two-of-five scheme in which two bits are binary ones and three are zeros. The four-bit space field uses a one-of-four scheme (one bit is a binary one and the rest are zeros). These schemes only produce 40 characters; therefore, four additional characters are obtained by encoding the five-bit bar field in a zero-of-five scheme (all bits are zeros) and the four-bit space field in a three-of-four scheme (three bits are binary ones).

The five-bit bar field is sequentially encoded by five bars and the four-bit space field is sequentially encoded by four spaces. Within the nine-bit character, the bars are the odd bits ($b_1, b_3, \ldots b_9$) and the spaces are the even bits (b_2, b_4, b_6, b_8). Each nine-bit character is separated by a space which does not contain data.

When producing bar codes, wide bars and wide spaces are both binary ones and should be equal in width. Narrow bars and spaces should be equal in width and both are binary zeros. Wide elements should be no less than two, but no more than three times the width of the narrow bar code elements. Intercharacter spaces should be no less than equal to, but no more than twice the narrow elements. High density bar codes (9.4 char/in.) should contain wide elements of no less than 2.24 times the width of narrow elements.

d. Three-of-Nine Encoding Data (See Tables A1 and A2)

The following charts present the bit pattern for the 44 characters recognized by this encoding scheme. Certain combinations will produce control characters recognized by the data terminal. The spaces are interleaved (even bits) between the bars and are presented in the chart above the bit pattern for the bars. These tables are included as an aid in the production of bar code labels.

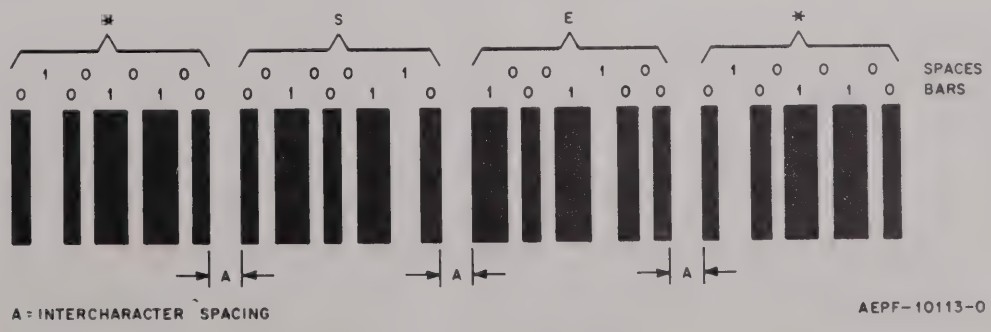


Figure A1. Code 39 Data Field

Radio Electrical Parts List PLF-1492-A

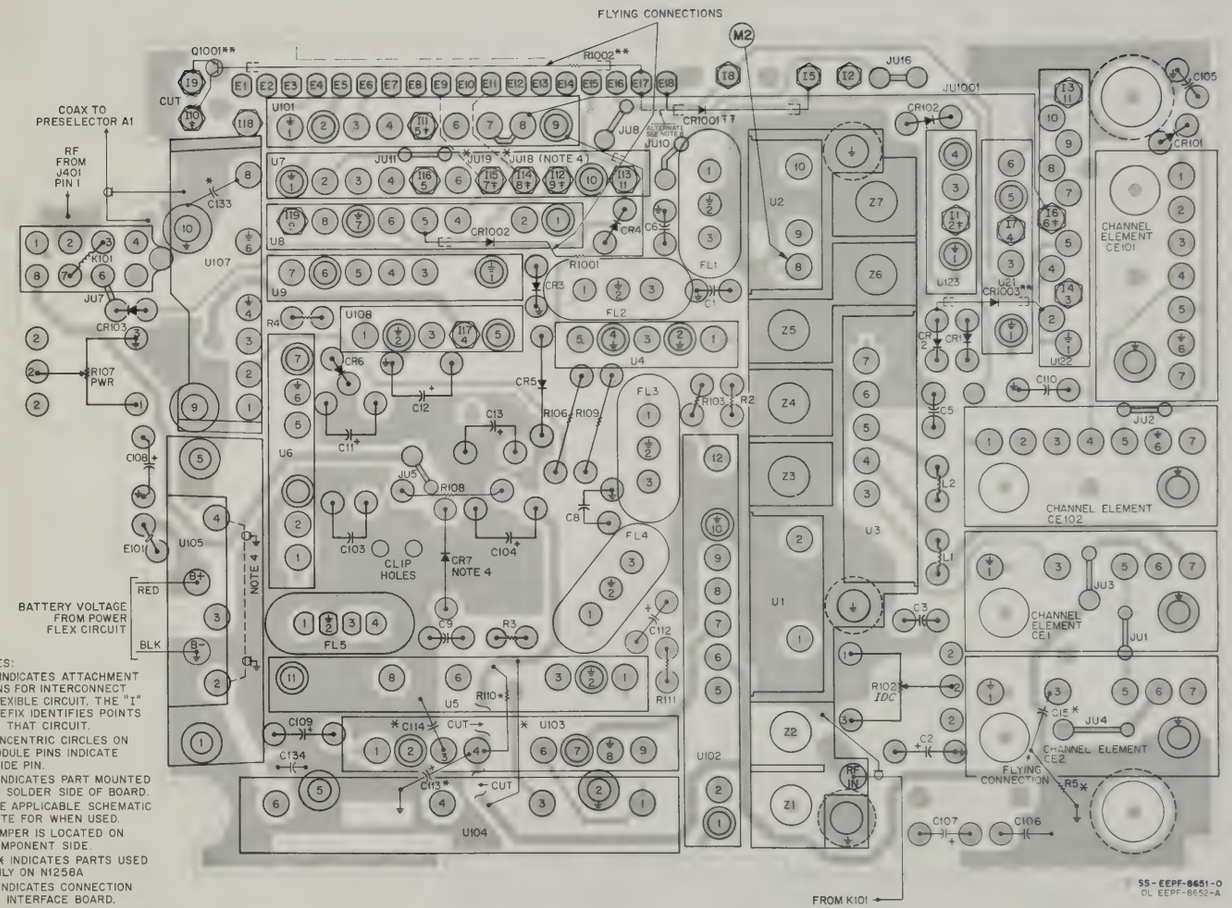
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		PRESELECTOR:
A1	NLE6931A	403-430 MHz; contains U1, U2, & U3
	or NLE6932A	440-470 MHz; contains U1, U2, & U3
	or NLE6933A	470-512 MHz; contains U1, U2, & U3
		CAPACITOR, Fixed: pF ±10%; 20 V unless stated
C1	2182358G96	30; 75 V; N150
C2	2382397D16	22 uF ±20%; 15 V
C3	2182358G95	30; 75 V; N750
C5	2182213E06	4700 ±20%; 100 V
C6	2182358G76	18.5 ±2%; 25 V
C8	2182358G76	18.5 ±2%; 25 V
C9	2184008H01	.01 uF; 50 V
C11, 12, 13	2382397D03	10 uF ±20%; 6 V
C15	2184008H14	4700; 100 V
C103	2184008H01	.01 uF; 50 V
C104	2382397D04	15 uF ±20%; 15 V
C105, 106	2182358G95	30; 75 V; N750
C107	2382397D03	10 uF ±20%; 6 V
C108	2382397D04	15 uF ±20%; 15 V
C109	2382397D15	10 uF ±20%
C110	2184008H01	.01 uF; 50 V
C112	2382397D09	6.8 uF ±20%; 10 V
C113	2382397D16	22 uF ±20%; 15 V
C114	2105311E49	30; 75 V; N750
C301	2382397D25	0.27 uF
C302	2382397D36	1 uF
C304	2382397D25	0.27 uF
C133, 134	2182358G01	3.3 pF ±0.25 pF; NPO
		CHANNEL ELEMENT:
CE1, 2	KXN1039B	Receiver, use as required
	or KXN1067B	(Used with expanded offset options)
CE101	NLE6975A	Transmitter, 21.4 MHz (0 MHz offset)
CE102	NLE6972A	Transmitter, 26.4 MHz (5 MHz offset)
	or NLE6973A	Transmitter, 24.4 MHz (3 MHz offset)
		DIODE: See Note
CR1 thru 6	4805824C01	Silicon
CR101, 102, 103	4805824C01	Silicon
CR301, 302	4805824C01	Silicon
CR303	4805504C01	LED
		CORE:
E101	2405913C04	Ferrite Bead
		FUSE:
F401	0105950E50	5-Amp. cartridge
		FILTER:
FL1/FL2	4805535C05	Matched pair; FL1 coded BLK, FL2 coded ORG
FL3/FL4	4805535C07	Matched pair; FL3 coded BLU, FL4 coded VIO
FL5	4805530C01	Discriminator, crystal, coded GRN
		JACK:
J301	0905537F01	Speaker, 2-conductor
J302	0905675C01	Socket, miniature accessory connector
J303	0105957D83	ASSEMBLY, Cable; Speaker-Microphone
J401	0905505C02	Antenna, 2-conductor
J402	1505673C01	Accessory Connector, housing portion; contains S401
		RELAY:
K101	8005037E01	8-pin DPDT
		COIL, RF: unless stated
L1, 2	2482723H04	Choke, 0.29 uH
		SPEAKER-MICROPHONE:
LS401/MK401	0105950E52	Assembly includes exploded view items 2, 7, and 9

NOTE: Since the diodes used in this radio are often selected for specific characteristics, replacement diodes should be ordered from Motorola using the Motorola part number listed to ensure optimum performance.

		RESISTOR, Fixed: Ω ±10%; 1/8 W unless stated
R2	0605139G10	47
R3	0600185B67	100
R4	0600185B73	330
R5	0600185B70	180
R102	1805310C01	pot. 10 k
R103	0600185B79	1 k
R106	0600185B83	2.2 k
R107	1805310C02	pot. 2 k
R108	0600185B83	2.2 k
R109	0600185B87	4.7 k
R110	0605139G02	4.7; 1/4 W
R111	0600185B85	3.3 k
R131	0600185A83	27 k ±5%
R132	0600185B80	1.2 k
R301	0605139G12	47 ±5%; 1/4 W
R306	0600185B73	330
R307	0600185B87	4.7 k
R308	1805602C02	pot. 50 k; contains S302
R309	0600185B76	560
R310	0600185B99	47 k
R311	1805430C02	pot. 25 k
R313, 314	0600185B91	10 k
		SWITCH:
S301	0105952E63	Rotary, 2-position, two-freq.
S302		ON/OFF, part of R308
S304	4082159D01	Sub-miniature, SPDT; push-to-talk
S401		p/o J402
		HYBRID, Encapsulated:
U1, 2, 3		p/o A1
U4	NLN8917A	First I-F Amplifier
U5	NLN8773A	Second I-F Amplifier
U6	NLN8774A	Discriminator
U7	NLN8777B	Audio Filter & Regulator
U8	NLN8775B	Audio Power Amplifier
U9	NLN8776A	Squelch
U101	NLN5832A	"IDC"
U102	NLE8342A	Phase Lock Loop Processor
U103	NLE8801A	VCO & Gate (403-430 MHz)
	or NLE8802A	VCO & Gate (440-470 MHz)
	or NLE8803A	VCO & Gate (470-512 MHz)
U104	NLE8181A	Power Amplifier (403-430 MHz)
	or NLE8182A	Power Amplifier (440-470 MHz)
	or NLE8183A	Power Amplifier (470-512 MHz)
U105	NLE8001A	Power Amplifier (403-430 MHz)
	or NLE8002A	Power Amplifier (440-470 MHz)
	or NLE8003A	Power Amplifier (470-512 MHz)
U107	NFE6001A	Filter & Detector (403-430 MHz)
	or NFE6002A	Filter & Detector (440-512 MHz)
U108	NLN8779A	Automatic Level Control
		DIODE: See Note
VR301	4883461E48	4.75 V Zener
		CABLE:
W1	0105952D58	Assembly, Coax

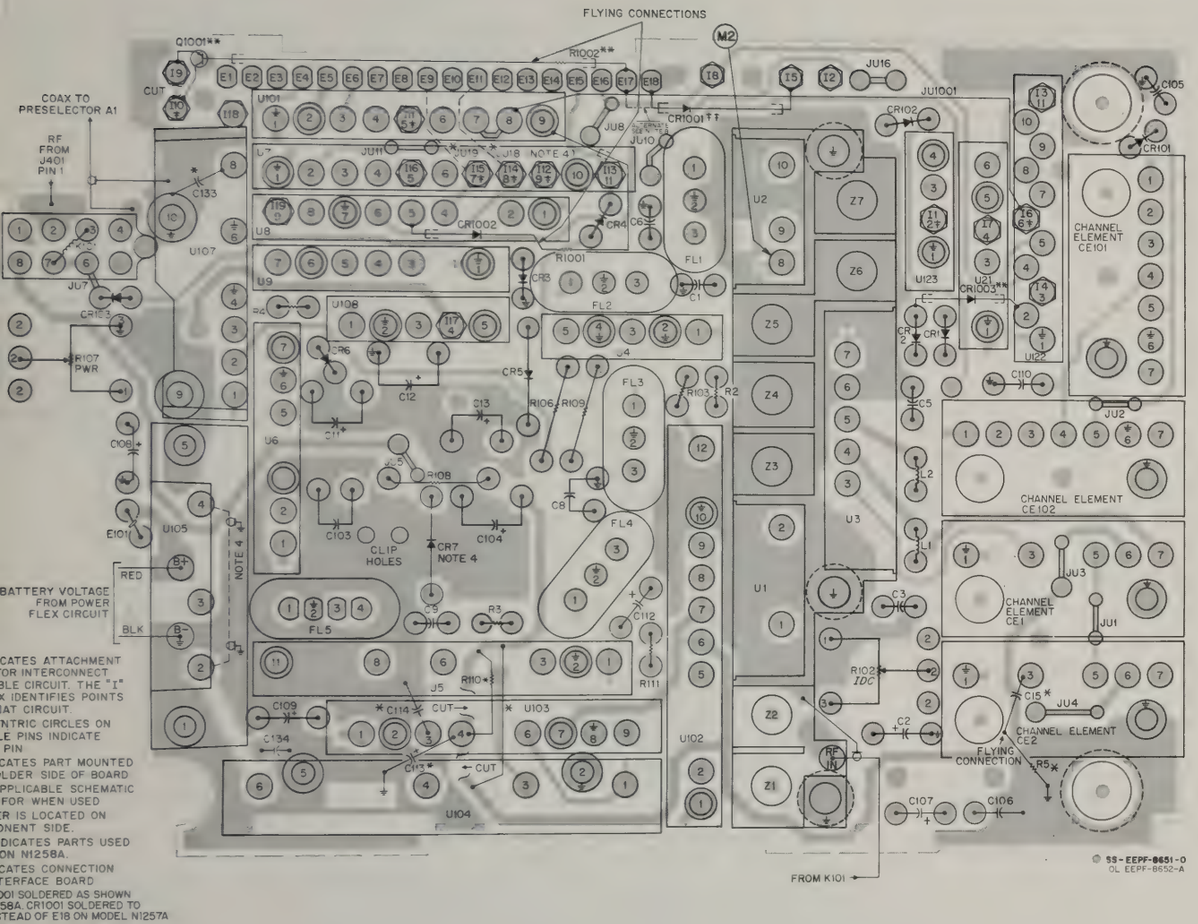
NONREFERENCED ITEMS

	0305628C01	SLUG and Mounting Stud for Preselector A1
	1405601C01	INSULATOR, for K101
	1405736C01	INSULATOR, for Crystal (3-spot) FL5
	7505295B01	PAD, for crystal FL1-FL4
	7605445C01	SLUG, for channel elements
	0705196A01	BOOT, Crystal FL1-FL5
	0705778D01	BOOT, for U108
	0905604C06	SOCKET, Guide Pin
	0905287C05	SOCKET, Module
	2205794E01	PIN, for option flex connection
	4705598C01	SOCKET, Post; option (e.g., I11-I17)
	4205360E01	CLIP, Grounding; for U102 can to preselector
	NAE6231A	ANTENNA, Helical UHF (400-440 MHz)
	NAE6232A	ANTENNA, Helical UHF (440-470 MHz)
	NAE6233A	ANTENNA, Helical UHF (470-512 MHz)
	0205863A01	NUT, for preselector
	0400115361	LOCKWASHER, for preselector
	0300139835	SCREW, for Filter U107
	0405683D01	LOCKWASHER, for Filter U107
	0400474215	WASHER, Insulating; for preselector
	2905254F01	LUG, Grounding; (between Antenna Jack J401 and P.C. Board)



NOTES:
1. ○ INDICATES ATTACHMENT PINS FOR INTERCONNECT FLEXIBLE CIRCUIT. THE "I" PREFIX IDENTIFIES POINTS ON THAT CIRCUIT.
2. CONCENTRIC CIRCLES ON MODULE PINS INDICATE GUIDE PIN.
3. * INDICATES PART MOUNTED ON SOLDER SIDE OF BOARD.
4. SEE APPLICABLE SCHEMATIC NOTE FOR WHEN USED.
5. JUMPER IS LOCATED ON COMPONENT SIDE.
6. ** INDICATES PARTS USED ONLY ON N1258A
7. † INDICATES CONNECTION TO INTERFACE BOARD.
8. †† CR1001 SOLDERED AS SHOWN ON N1258A. CR1001 SOLDERED TO E17 INSTEAD OF E18 ON MODEL N1257A

Figure 51. Radio Section, Main Circuit Board Component Layout Diagram and Parts List



72 *Figure 51. Radio Section, Main Circuit Board Component Layout Diagram and Parts List*

APPENDIX A

1. INTRODUCTION

The purpose of this section is to define the three-of-nine (3/9) bar code and to provide a guide for the production of the bar code media. This reference is intended only as a guide, since media quality depends upon the discretion of the ultimate user.

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Scan rate is to a degree a function of the physical size of the media being scanned. Media, whose widest module (bar or space) is no wider than 0.37 inches, can utilize the full three to thirty inches/second scan rate range of the data terminal. Larger media increases the minimum acceptable scan speed; i.e., modules with a 0.1 inch width require a minimum scan speed of approximately 8 inches/second.

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This code provides a set of 44 unique combinations (characters) based on nine bits for each character. Three of the nine bits are binary ones and the remainder are zeros. The three-of-nine code is used to sequentially encode an unlimited string of characters. A start/stop character ("*") provides for positive recognition of the beginning and the end of the data string. The start/stop character decodes to an asterisk (Hex ASCII Code 2A) and can be used in the bar coded data string if the asterisk character is desired.

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The following charts present the bit pattern for the 44 characters recognized by this encoding scheme. Certain combinations will produce control characters recognized by the data terminal. The spaces are interleaved (even bits) between the bars and are presented in the chart above the bit pattern for the bars. These tables are included as an aid in the production of bar code labels.

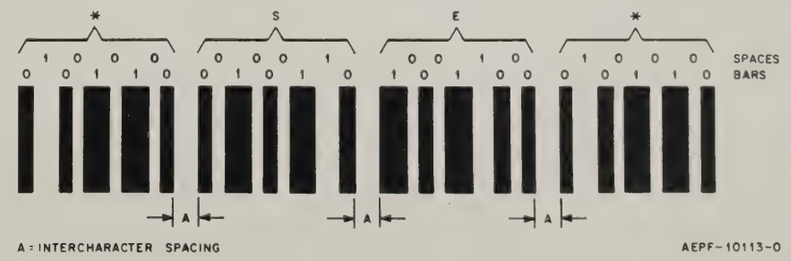

Figure A1. Code 39 Data Field

Table A1. Binary 3/9 Code Table

	b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8	b_9		b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8	b_9	
1	1	0	0	1	0	0	0	0	1	Spaces 1/4 Bars 2/5	0	0	0	0	1	1	0	0	1	D
2	0	0	1	1	0	0	0	0	1		1	0	0	0	1	1	0	0	0	E
3	1	0	1	1	0	0	0	0	0		0	0	1	0	1	1	0	0	0	F
4	0	0	0	1	1	0	0	0	1		0	0	0	0	0	1	1	0	1	G
5	1	0	0	1	1	0	0	0	0		1	0	0	0	0	1	1	0	0	H
6	0	0	1	1	1	0	0	0	0		0	0	1	0	0	1	1	0	0	I
7	0	0	0	1	0	0	1	0	1		0	0	0	0	1	1	1	0	0	J
8	1	0	0	1	0	0	1	0	0		1	0	0	0	0	0	0	1	1	K
9	0	0	1	1	0	0	1	0	0		0	0	1	0	0	0	0	1	1	L
0	0	0	0	1	1	0	1	0	0		1	0	1	0	0	0	0	1	0	M
A	1	0	0	0	0	1	0	0	1		0	0	0	0	1	0	0	1	1	N
B	0	0	1	0	0	1	0	0	1		1	0	0	0	1	0	0	1	0	O
C	1	0	1	0	0	1	0	0	0		0	0	1	0	1	0	0	1	0	P
Q	0	0	0	0	0	0	1	1	1		0	1	0	0	1	0	0	0	1	X
R	1	0	0	0	0	0	1	1	0		1	1	0	0	1	0	0	0	0	Y
S	0	0	1	0	0	0	1	1	0		0	1	1	0	1	0	0	0	0	Z
T	0	0	0	0	1	0	1	1	0		0	1	0	0	0	1	0	0	1	–
U	1	1	0	0	0	0	0	0	1		1	1	0	0	0	1	0	0	0	
V	0	1	1	0	0	0	0	0	1		0	1	1	0	0	0	1	0	0	SP (SPACE)
W	1	1	1	0	0	0	0	0	0		0	1	0	0	1	0	1	0	0	* (Start/Stop)
$	0	1	0	1	0	1	0	0	0	Spaces 3/4 Bars 0/5	0	1	0	0	0	1	0	1	0	+
/	0	1	0	1	0	0	0	1	0		0	0	0	1	0	1	0	1	0	%

Table A2.
Control Code and Punctuation Mark Symbol Assignments

FUNCTION	CODE 3/9 SYMBOLS
INSERT	* $ $ *
ON	* $ / *
BRT	* $ + *
DIM	* $ % *
DELETE	* / $ *
CL - M	* / / *
PA	* / + *
CL - I	* / % *
BACKSPACE	* + $ *
TAB RIGHT	* + / *
ENTER	* + + *
TAB LEFT	* + % *
FORWARD SPACE	* % $ *
CL - F	* % / *
PF	* % + *
RESET	* % % *
APOSTROPHE	* SP $ *
COMMA	* SP / *
QUESTION MARK	* SP + *
EQUAL SIGN	* SP % *

NOTES:
1. SP = SPACE
2. The apostrophe, comma, question mark, and equal sign do not have unique code 39 symbols to represent them, so they are encoded using a space followed by one of the special characters ($, %, +, /). These two-character sequences can be included in a line of bar coded data, and will be recognized as punctuation marks. Therefore it follows that it is not possible to encode a space followed by a dollar sign, or any of the other three combinations, and have the terminal recognize them as such.

MOTOROLA

MANUAL USER QUESTIONNAIRE

We believe that reports from users provide valuable information for producing good service manuals. Your answers and comments on the following questionnaire will aid us in writing manuals that contain information of maximum benefit to you.

In reference to Manual No. 68P_____

DIAGRAMS (indicate diagram number/description) _____

_____

☐ Are adequate

☐ Are too small ☐ too big

☐ Should contain the following additional information: _____

_____

☐ Contain the following errors: _____

_____

PARTS LISTS

☐ Are adequate

☐ The following information is incorrect or should be added: _____

_____

☐ I prefer exploded views for parts identification

THEORY/TROUBLESHOOTING INFORMATION

Fold down to this line

☐ I use troubleshooting charts frequently.

☐ I do not use troubleshooting charts.

☐ I prefer tabular symptom/remedy charts.

☐ The following information should be added (or corrected): _____

_____

MODEL CHARTS

☐ I use charts to determine if manual is applicable to my radio model.

☐ I use the charts to determine content of model or identify what chassis/ kits are in the model; or: _____

_____

☐ I do not use these charts.

PRINTED CIRCUIT BOARD DETAILS

EPF-10123-O

- ☐ I use printed circuit details for component location only.
- ☐ In addition to component location, I use printed circuit details for: _____
  _____
- ☐ I prefer photographs/drawings with call-outs for component location purposes.
- ☐ Different shades of gray are adequate for double-sided boards.
- ☐ I prefer use of different colors for double-sided boards.

OTHER COMMENTS

_____

_____

My name is _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone no. (include area code) _____

Please fold carefully so that bar pattern can be read by postal service optical scanner equipment

No Postage Stamp Necessary if Mailed in the United States

BUSINESS REPLY MAIL

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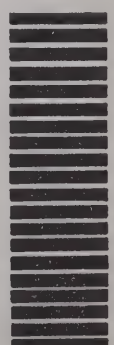

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REPLACEMENT PARTS ORDERING

ORDERING INFORMATION

Motorola's Communications Parts organization maintains a number of area parts offices conveniently located throughout the United States to handle domestic orders. These facilities are staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola communications products.

Orders for all parts **except** crystals, active filters, PROMs, channel elements, and Vibrasender® and Vibrasponder® resonant reeds should be sent to the nearest area parts office. Orders for instruction manuals should also be sent to the area parts office.

When requesting replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis. If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it. Replacement orders for programmed code plugs must also include all information on the existing code plug label.

Orders for crystals, channel elements, active filters, PROMs, and resonant reeds should be sent directly to the Component Products Sales & Service address. Crystal and channel element orders should specify the crystal or channel element type number, crystal and carrier frequencies, and the model number in which the part is used. Active filter, PROM, and resonant reed orders should specify type number and frequency, identify the owner/operator of the communications system in which these items are to be used, and include any serial numbers stamped on the components being replaced.

FACTORY ADDRESS FOR ORDERING CRYSTALS, CHANNEL ELEMENTS, ACTIVE FILTERS, PROMs, AND RESONANT REEDS

Motorola, Inc.
Component Products Sales & Service
P.O. Box 66191
O'Hare International Airport
Chicago, IL 60666

Street Address:
2553 N. Edgington Street
Franklin Park, IL 60131
Tel: 312-451-1297, TWX: 901-227-0799

AREA PARTS OFFICE

Western Area Parts
1170 Chess Drive, Foster City, CA 94404
Tel: 415-349-8621, TWX: 910-375-3877

Pacific Southwestern Area Parts
P.O. Box 85036, San Diego, CA 92138

Street Address:
9980 Carroll Canyon Road, San Diego, CA 92131
Tel: 714-578-8030, TWX: 910-335-1516

Gulf States Area Parts
P.O. Box 73115, 1140 Cypress Station, Houston, TX 77090
Tel: 713-537-3636, TWX: 910-881-6392

Southwestern Area Parts
P.O. Box 34290, 3320 Belt Line Road, Dallas, TX 75234
Tel: 214-620-8511, TWX: 910-860-5505

Midwest Area Parts
1313 E. Algonquin Rd., Schaumburg, IL 60196
Tel: 312-576-7430, TWX: 910-693-0869

Southeastern Area Parts
P.O. Box 368, Decatur, GA 30031

Street Address:
5096 Panola Industrial Blvd., Decatur, GA 30032
Tel: 404-987-2232, TWX: 810-766-0876

Rocky Mountain Area Parts
20 Inverness Place East, Englewood, CO 80112
Tel: 303-741-2323, TWX: 910-935-0785

East Central Area Parts
12955 Snow Road, Parma, OH 44130
Tel: 216-433-1560, TWX: 810-427-9424

Eastern Area Parts
85 Harristown Road, Glen Rock, NJ 07452
Tel: 201-444-9662, TWX: 710-988-5614

Mid-Atlantic Area Parts
7230 Parkway Drive, Hanover, MD 21076
Tel: 301-796-8763, TWX: 710-862-1941

National Accounts
Railroads, Airlines, and Telephone Sales
1313 E. Algonquin Road, Schaumburg, IL 60196
Tel: 312-576-6512, TWX: 910-693-0869

Motorola National Data Services
1711 West 17th Street, Tempe, AZ 85281
Tel: 602-994-6472, TWX: 910-951-1334

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